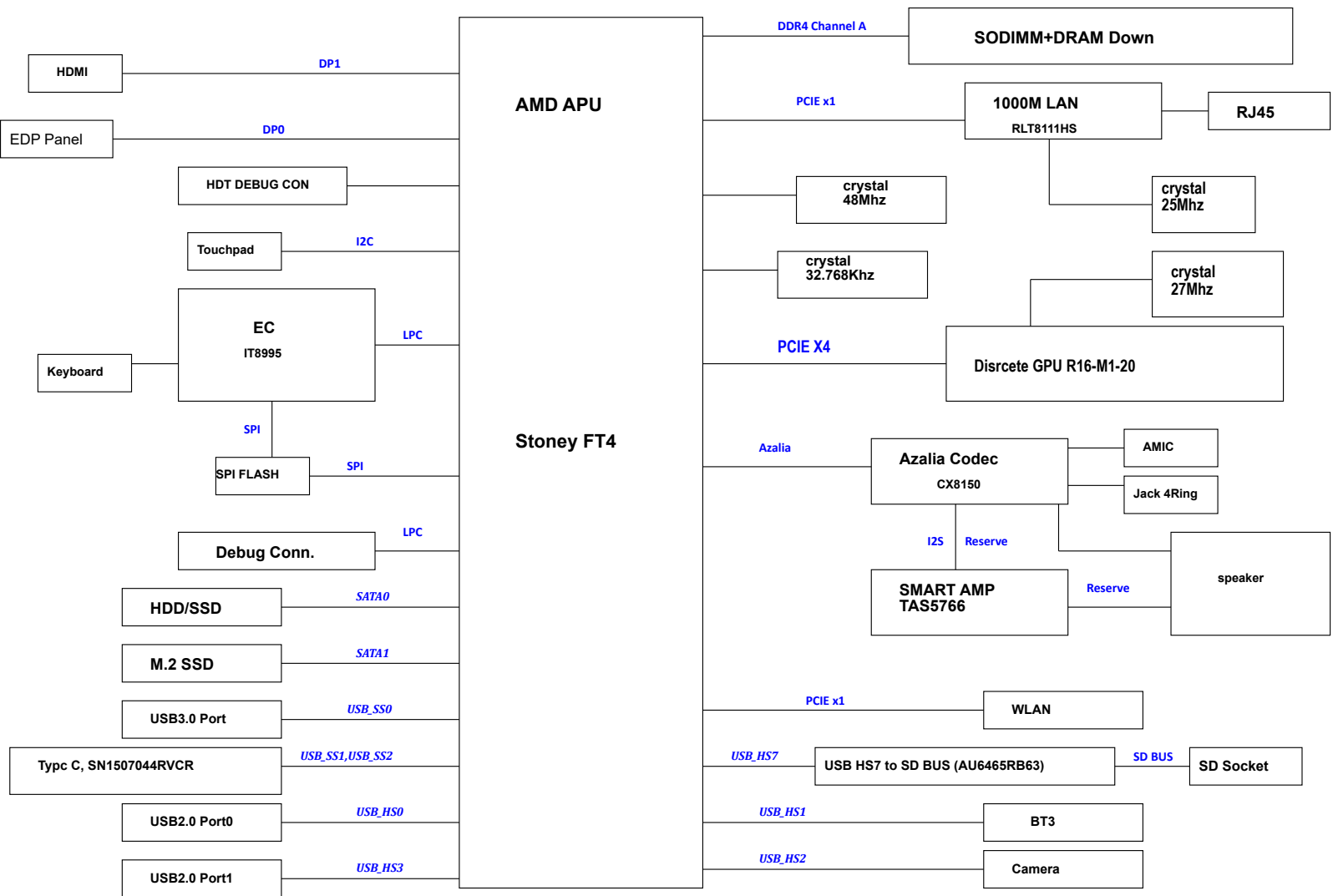


# X505B Schematic R1.0




<Variant Name>

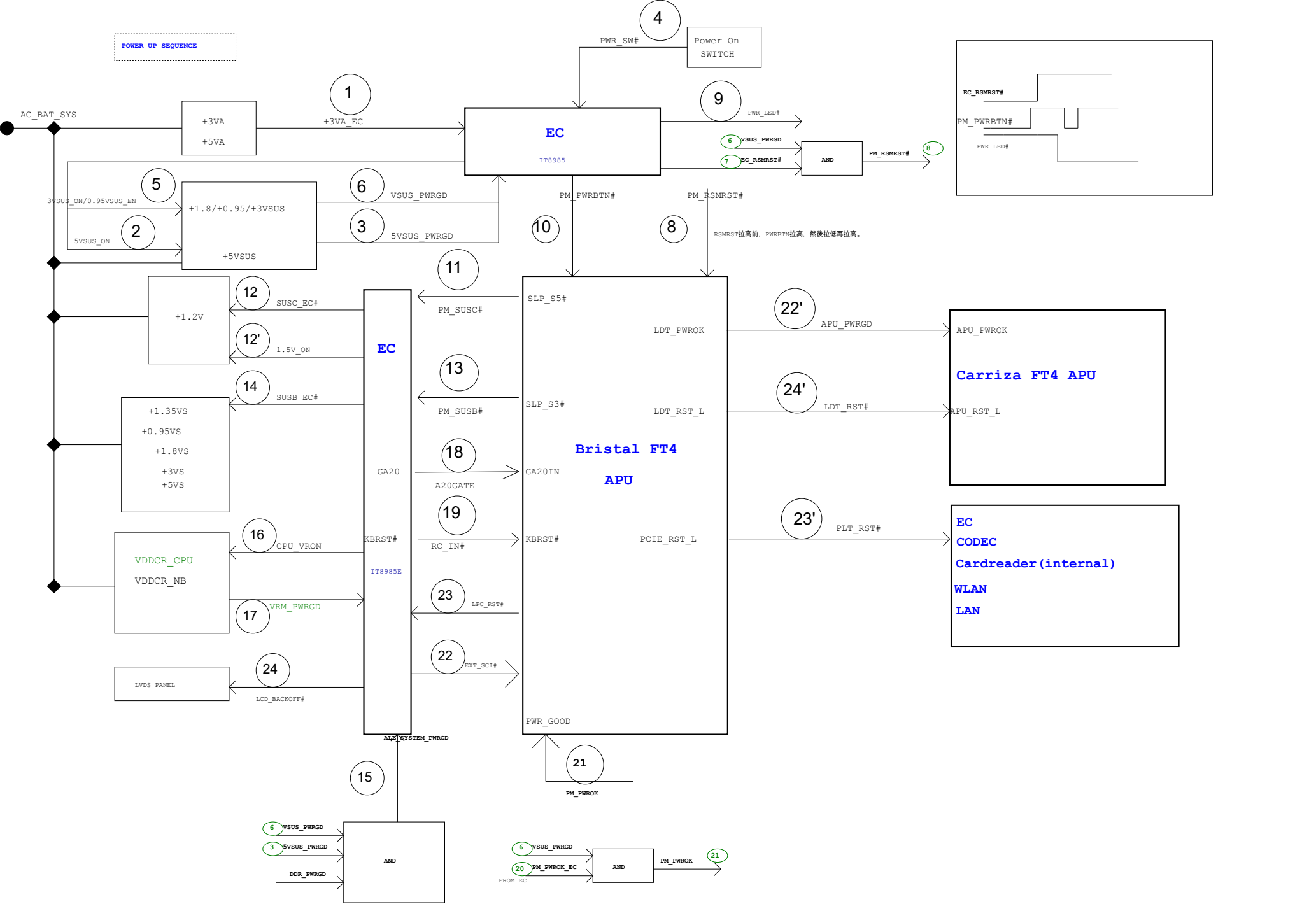
BOM PN	CPU	GPU	DRAM	VRAM	adapter w
60NB0E50-MB3010	A9-9400	R16M1-20	8G	SAM 2G	65W
60NB0E50-MB2010	A6-9200	R16M1-20	4G	MIC 2G	65W
60NB0E50-MB2110	E2-9000	R16M1-20	4G	MIC 2G	65W

1. EDP Connector Swap AUXP/N, 0828
2. DGPU\_RST# change to AGPIO85, 0828
3. PCBIID change to PU +1.8VS, 0828
4. SMBI change to PU +3VA\_EC, 0828
5. Del RN1803, RN1814, 0828
6. WLAN Power change to +3VS, 0829

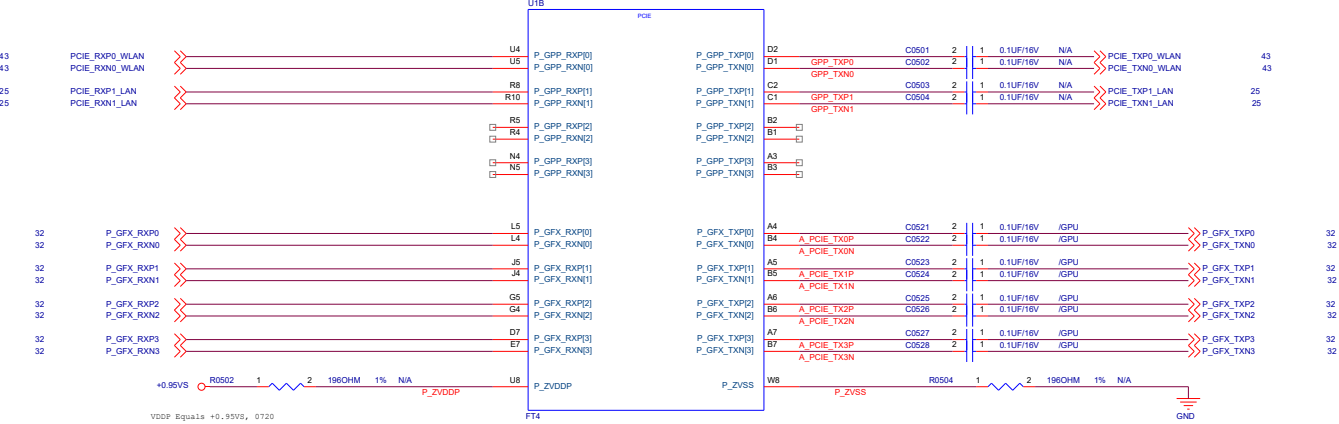
Update NTC3527U footprint, 1020  
SDDATA[0..3] add 39PF cap. 1026  
C2529,C2530,C3225,C3226,C4408,C4409 change to 4.7PF, 1026  
RN3301 change from N/A to /GPU, 1026  
PC9134 change from N/A to /GPU, 1027

<Variant Name>


		Project Name	Rev
		X505BP	R1.0
Title :			
Size	Dept.: NB-SZ-SYS1 Engineer:		
A			
Date: Thursday, March 30, 2017			Sheet 3 of 99

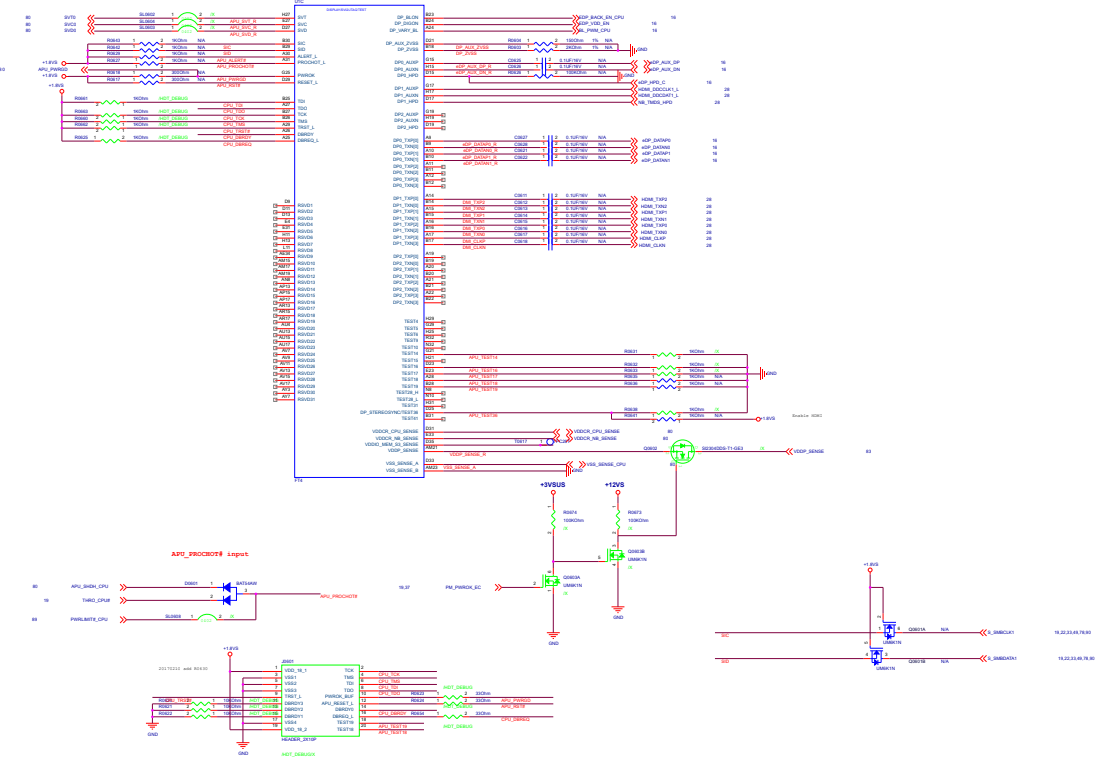


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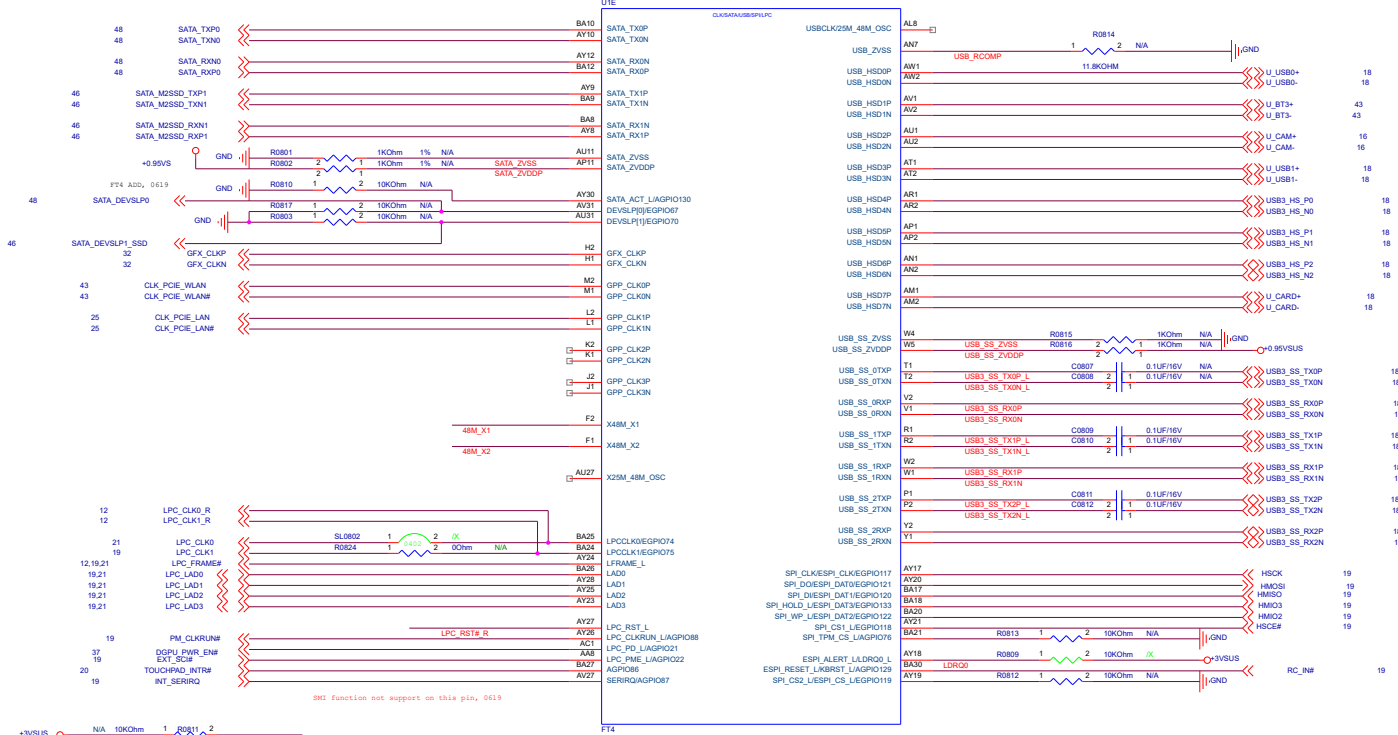
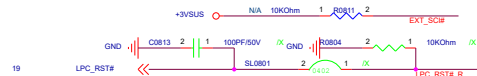


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Title :			
Size <b>C</b>	Dept.: <b>NB-SZ-SYS1</b>	Engineer:	
Date: <b>Thursday, March 30, 2017</b>	Sheet <b>5</b>	of <b>99</b>	










<Variant Name>

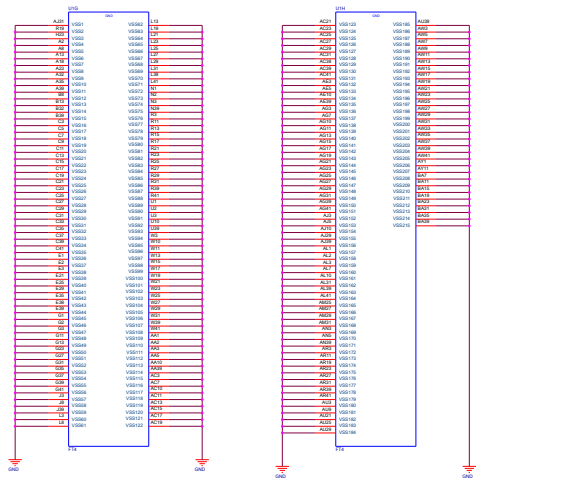
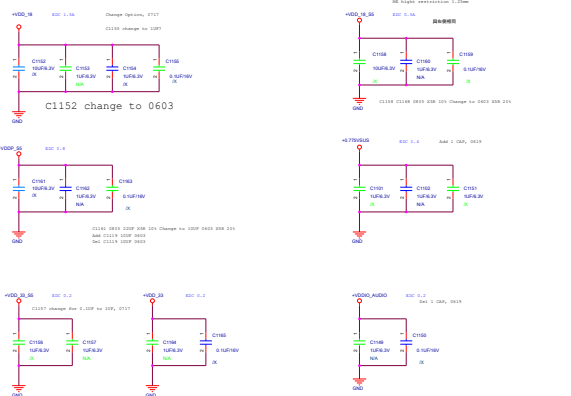
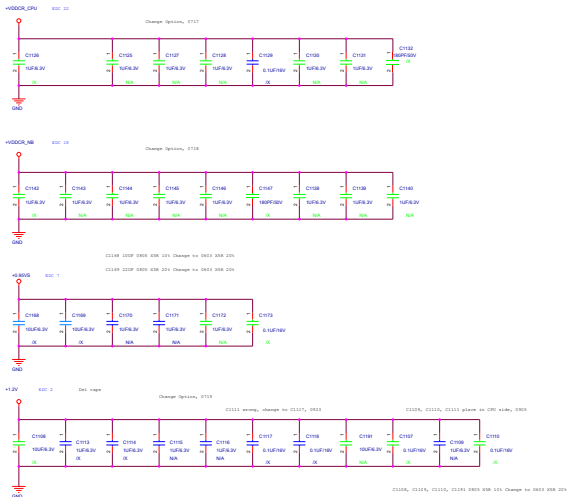
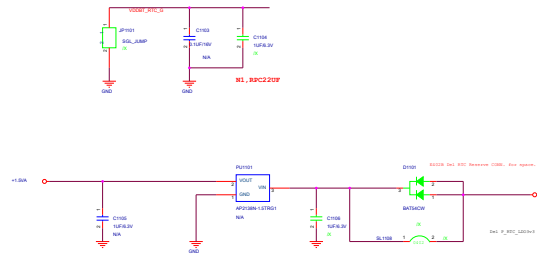
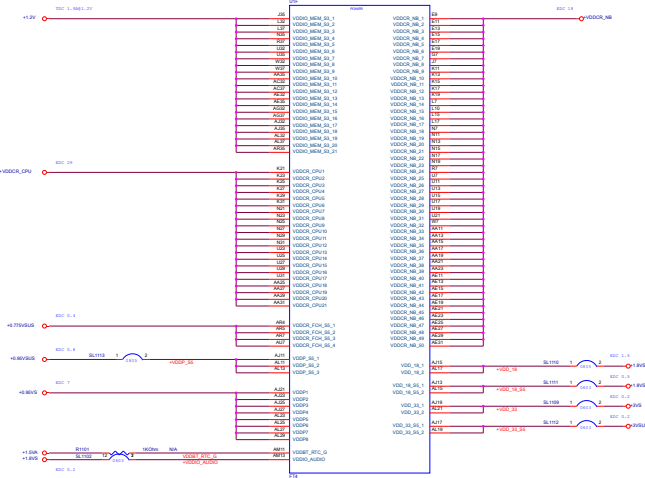
	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>C</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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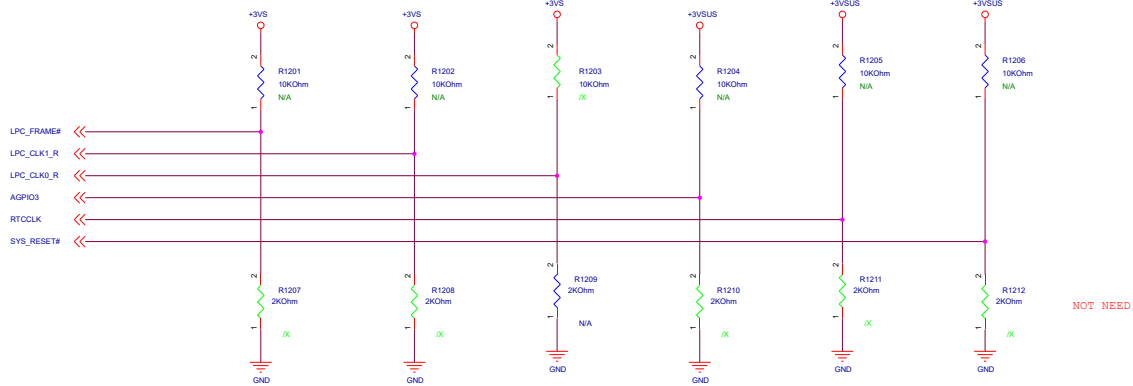
Date: <b>Thursday, March 30, 2017</b>	Sheet <b>9</b> of <b>99</b>
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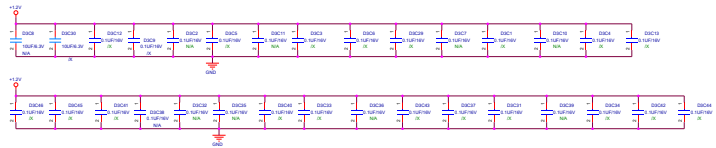
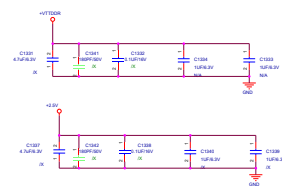
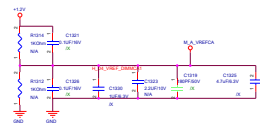
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8  
8  
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7  
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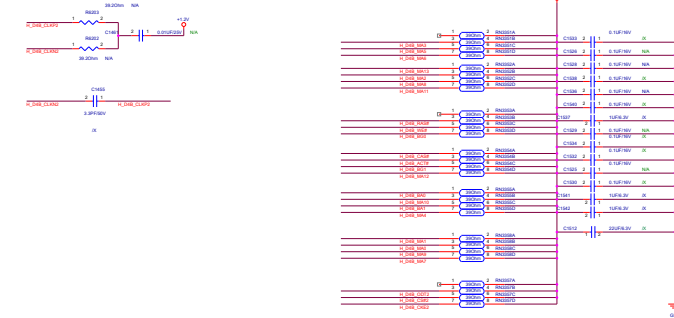
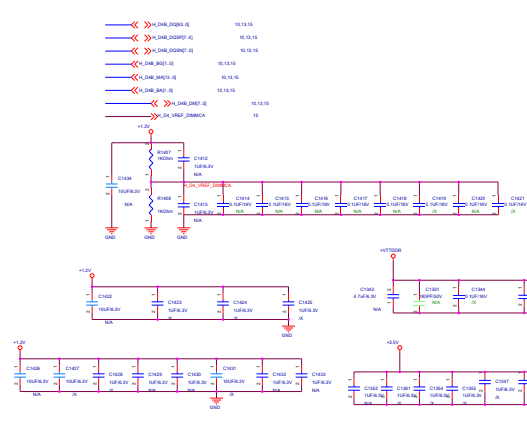


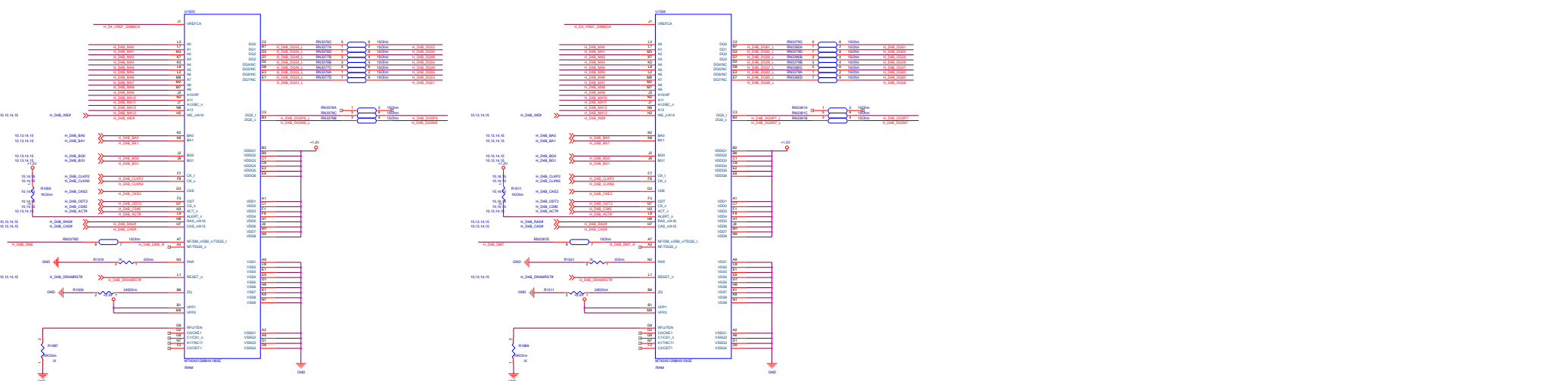
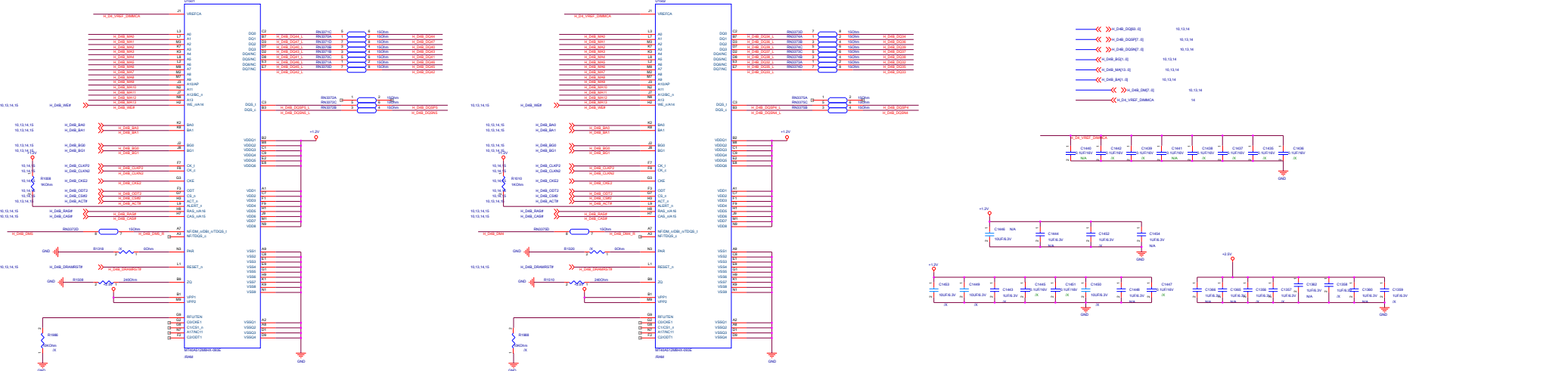
	LPC_FRAME#	LPC_CLK1_R	LPC_CLK0_R	AGPIO3	RTCCLK	SYS_RESET#
PULL HIGH	SPI ROM DEFAULT	configured for internal clock generator DEFAULT	Boot Fail Timer Enabled	Enhanced reset logic (CE only) DEFAULT	RTC coin battery is implemented DEFAULT	Normal powerup/reset timing DEFAULT
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled DEFAULT	Traditional reset logic	RTC coin battery is not implemented	Reserved

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<Variant Name>








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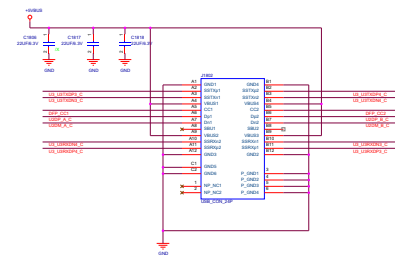
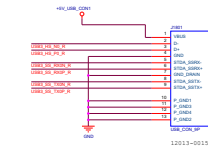
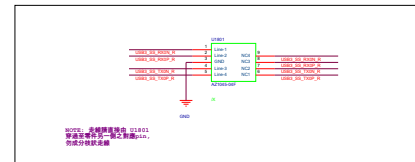
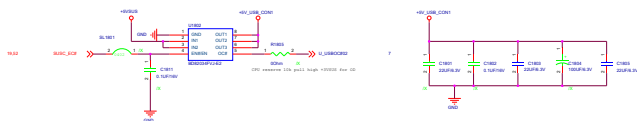




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20160503	17	D1701	Del SATA_ODD whole page	Smith

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		Project Name	Rev
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Title :			
Size			
C	Dept.:	NB-SZ-SYS1	Engineer:
Date: Thursday, March 30, 2017		Sheet	17 of 99

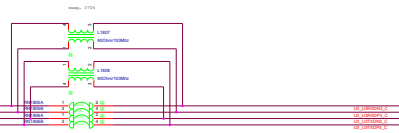


DFF CC Pull-Up Requirement for USB Type-C Power Options

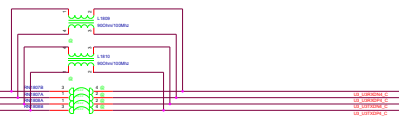
VBUS Power	CC Pull-Up (4.75-5.5V)	CC Pull-Up (3.3V +/- 5%)
Default USB Power	56k Ohm +/-20%	36k Ohm +/-20%
1.5A @ 5V	12k Ohm +/-5%	12k Ohm +/-5%
3.0A @ 5V	10k Ohm +/-5%	4.7k Ohm +/-5%

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	S1D	1.57 A	NA
0	1	S1D	1.57 A	NA
1	0	1.5 A	1.57 A	NA
1	1	3.0 A	3.34 A	1.77 A

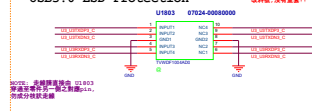
USB3.0 Bus



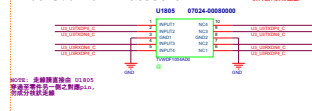
USB3.0 Bus



USB3.0 ESD-Protection



USB3.0 ESD-Protection



ECMF 20170208

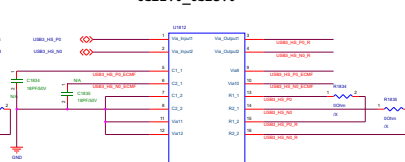
USB2.0\_TPYEC



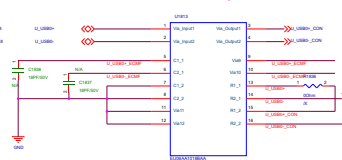
USB2.0\_TPYEC



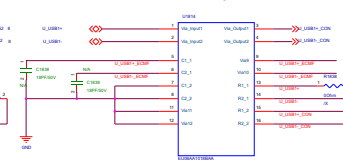
USB2.0\_USB3.0



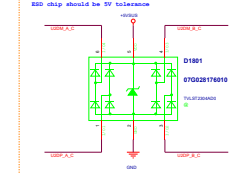
connected to USB 2.0 port



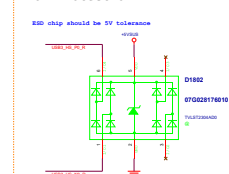
connected to USB 2.0 port



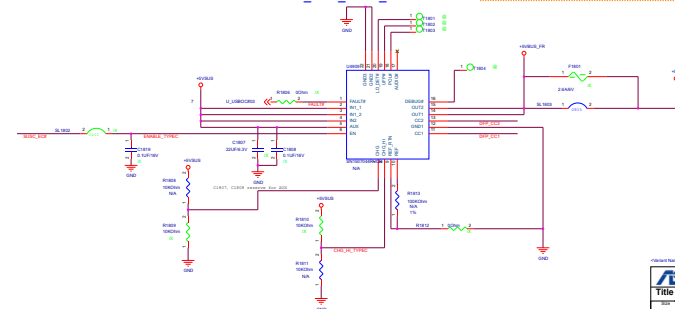
USB2.0 ESD-Protection

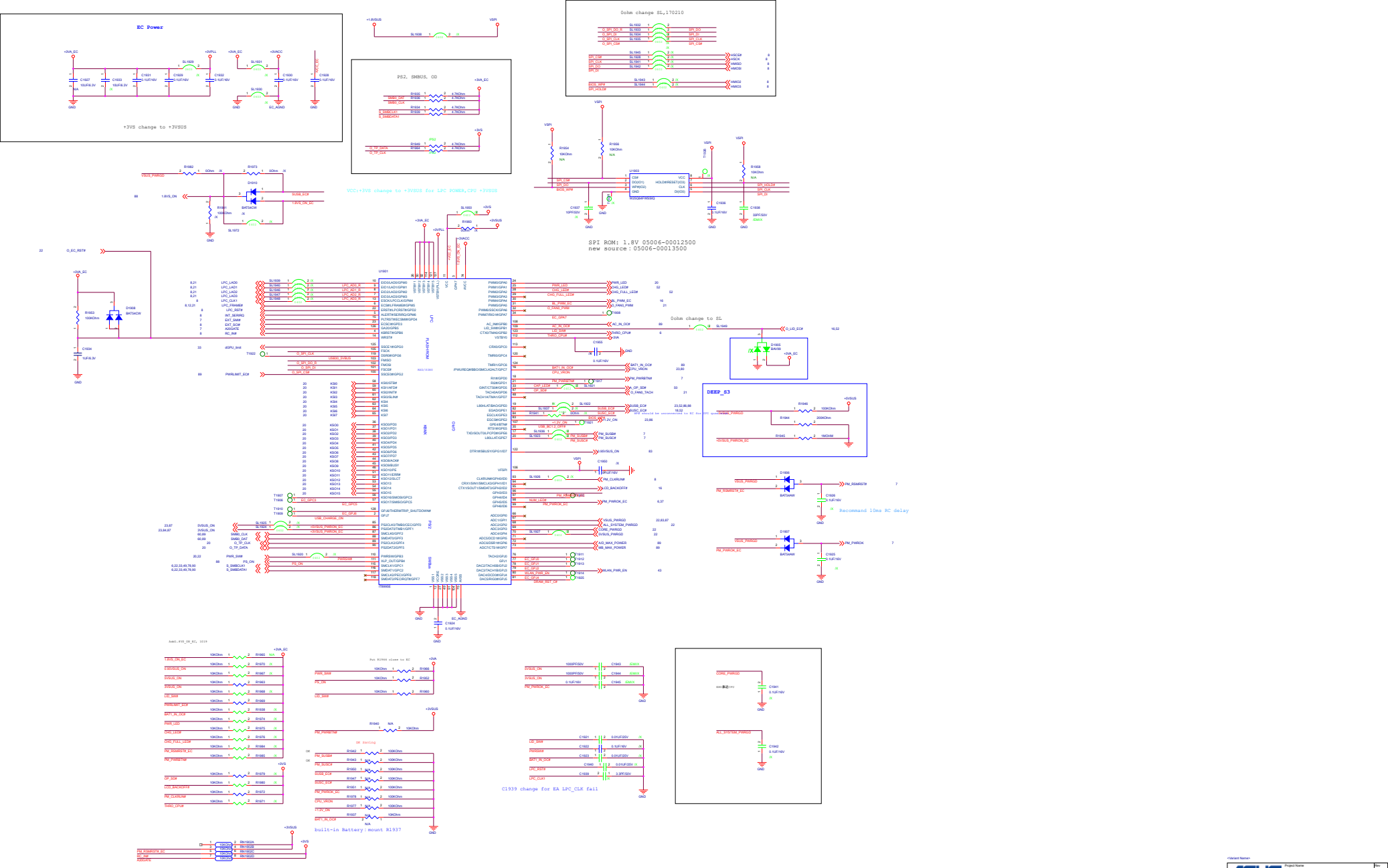


USB3.0/USB 2.0 ESD-Protection



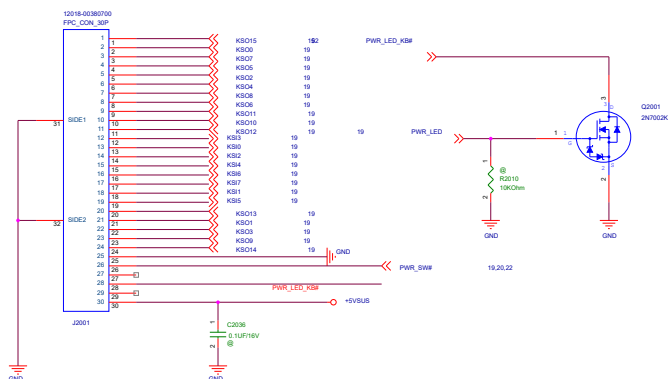
USB3\_Port\_Power\_Switch



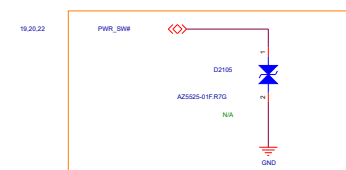
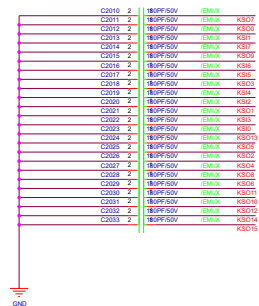


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## Keyboard Connector

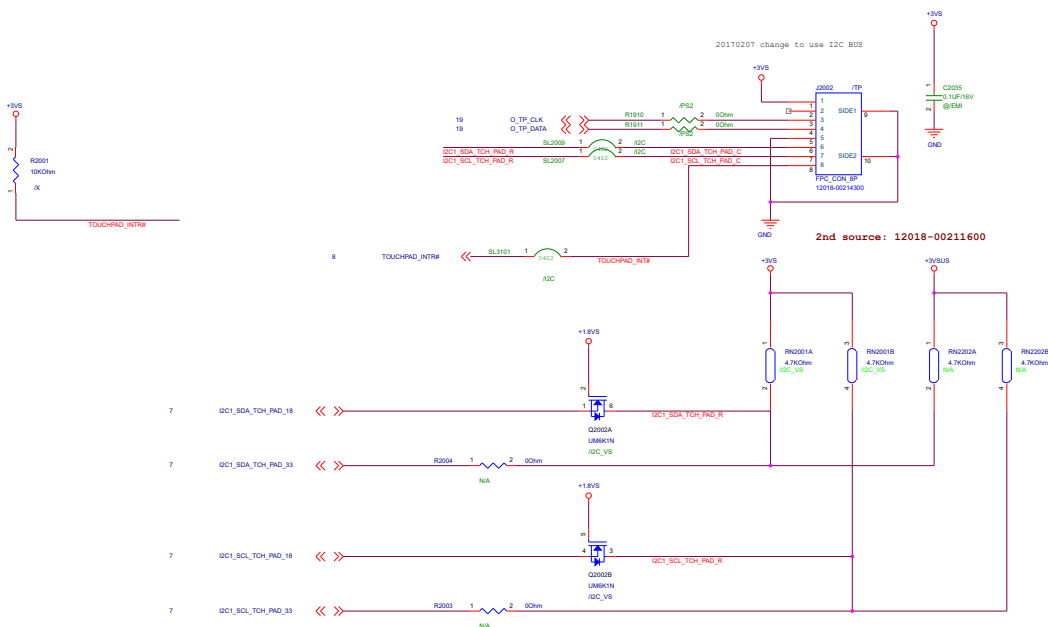


Reserved for EMI

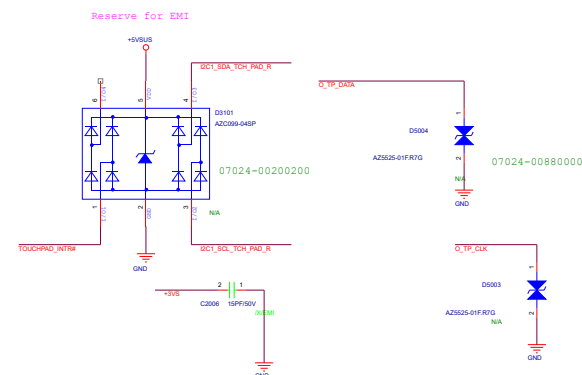


### For Touchpad Connector

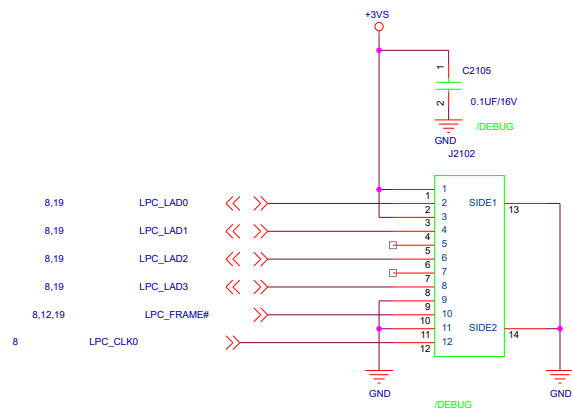
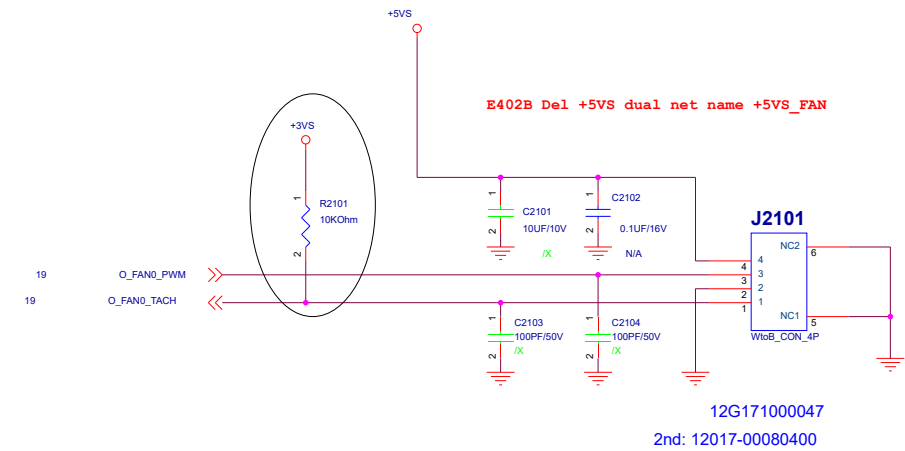
## TouchPad Connector

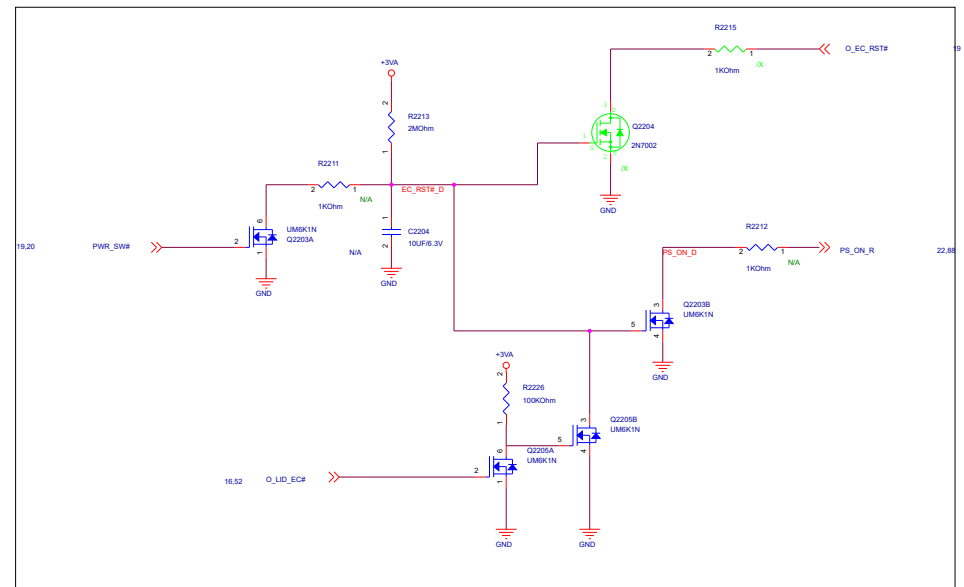
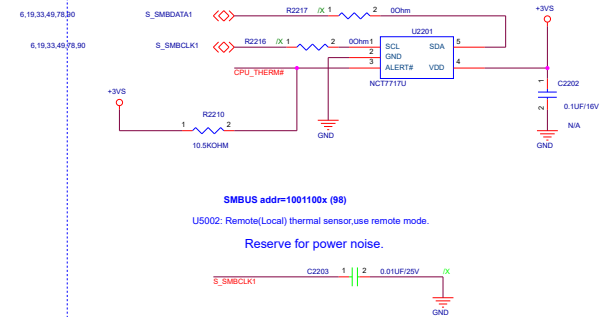
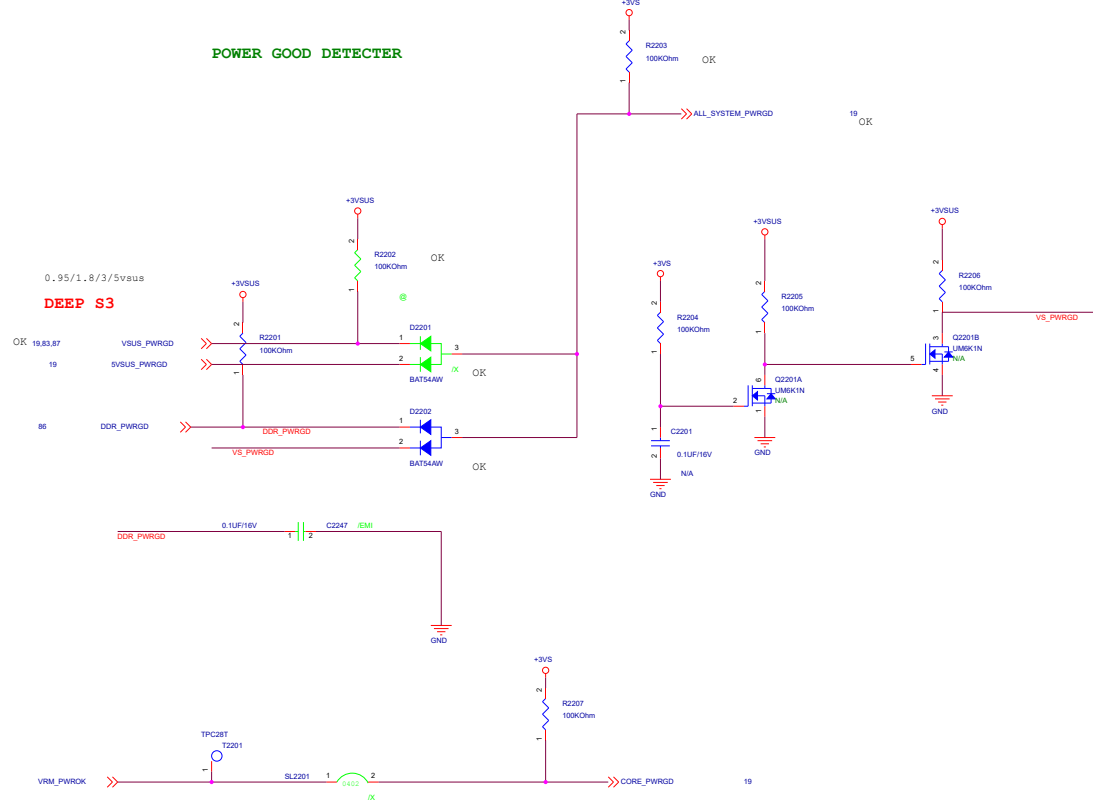


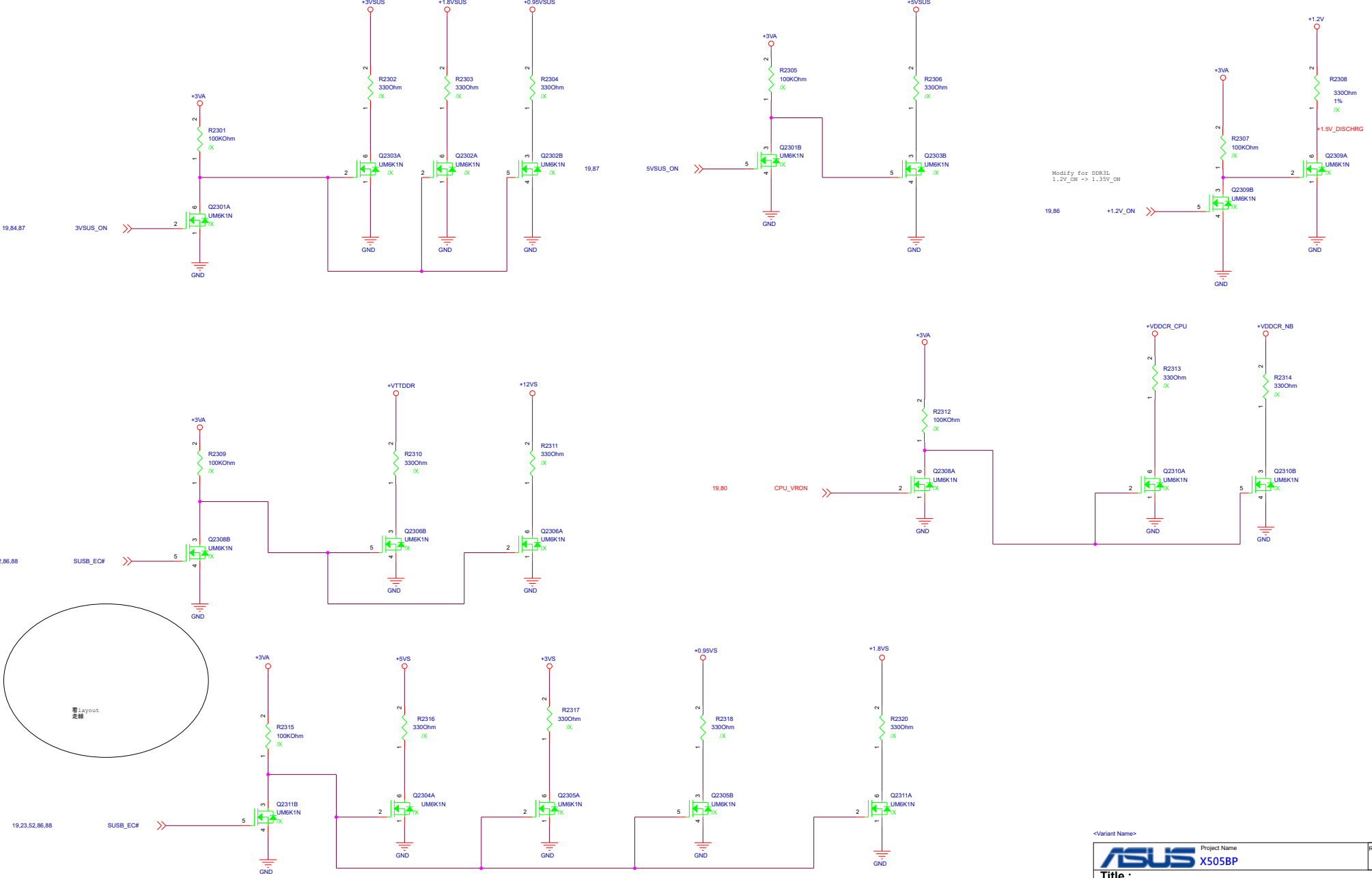
	F	I
	PIN NO.	PIN DEFINE*
	1	VDD_3.3V
	2	NC
	3	D-
	4	D+
	5	GND
	6	I2C_DATA
	7	I2C_CLK
	8	TOUCH -INT*



DC FAN Control








<Variant Name>

ASUS		Project Name	Rev
X505BP			R1.0
Title :			

Size	Dept.:	Engineer:	
A3	NB-SZ-SYS1		
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<Variant Name>

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**Title :**


Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>C</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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<Variant Name>

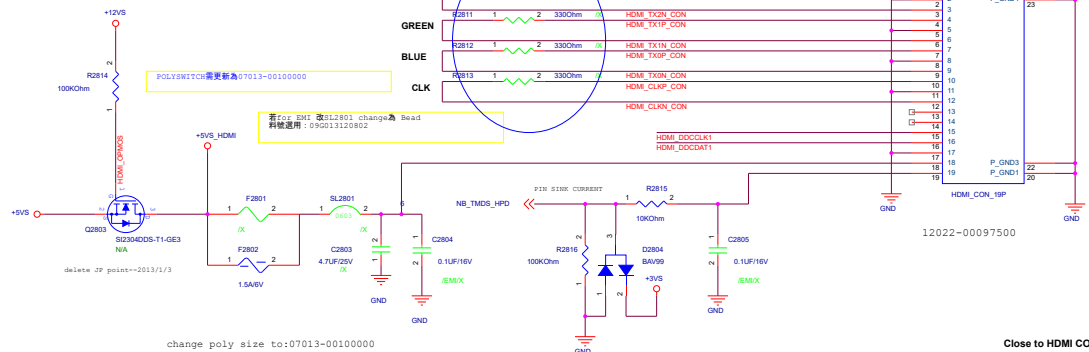
	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

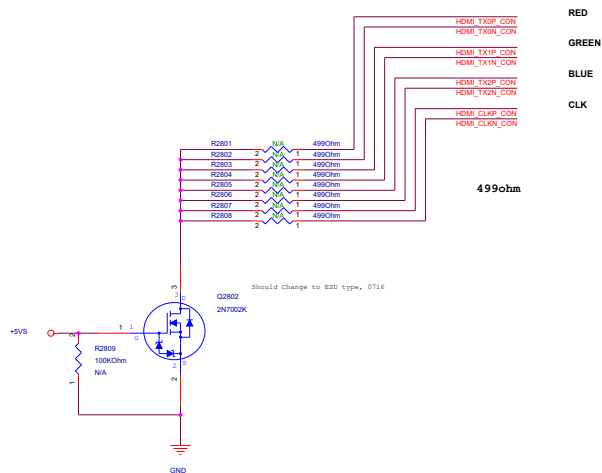
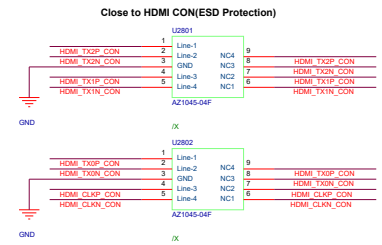
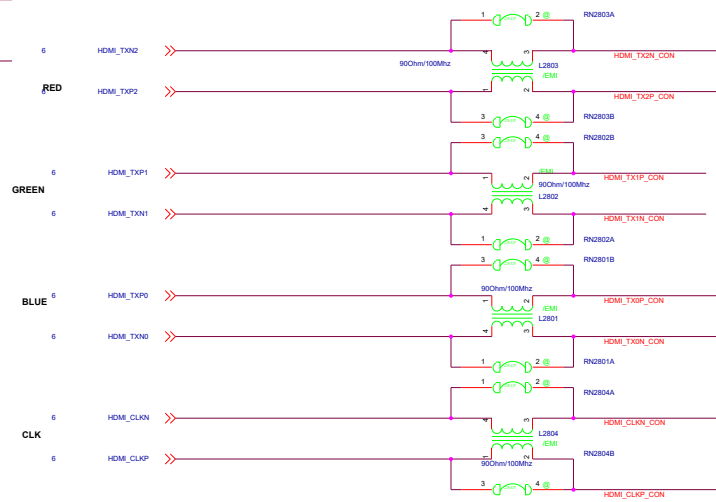
Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Should Change to KSD type, 0716




change poly size to:07013-00100000




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Date	Page	Type	Dscription	Author
20160508	29	D0601	Del CRT PTN3356 all sheet	Smith

<Variant Name>

		Project Name <b>X505BP</b>	Rev R1.0
<b>Title :</b>			
Size Custom	<b>Dept.:</b> NB-SZ-SYS1		<b>Engineer:</b>
Date: Thursday, March 30, 2017		Sheet	29 of 99

<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>30</b> of <b>99</b>
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<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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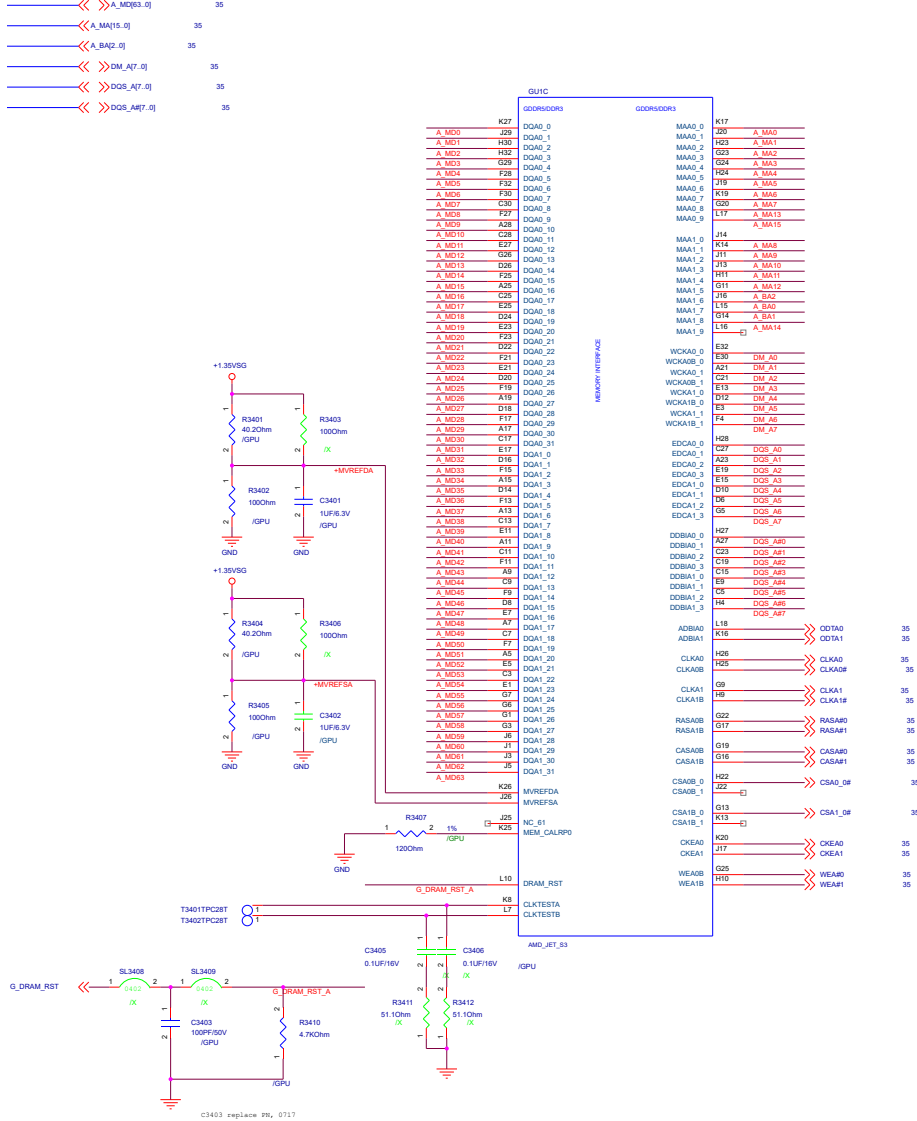
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<Variant Name>



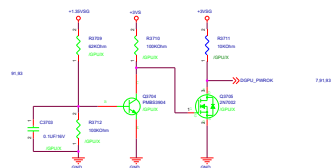
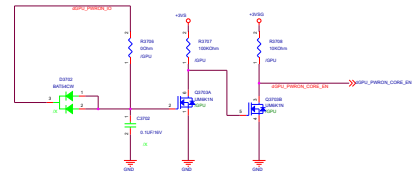
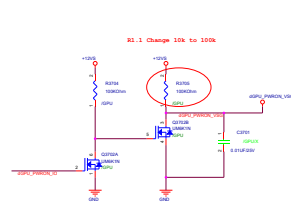
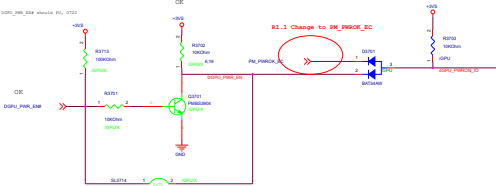




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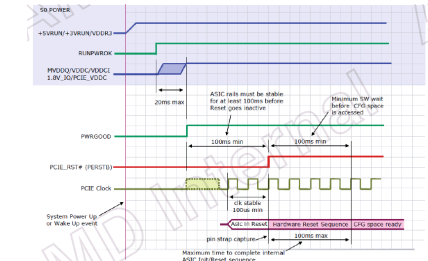


## GPU 電源供電時序

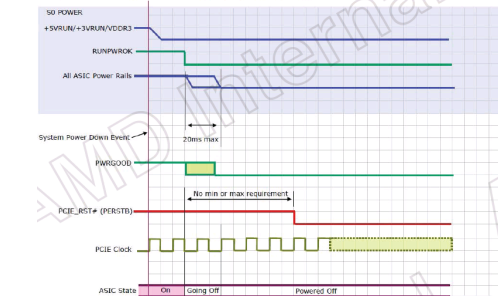
"Solar" GPU電源供電時序要求所有電源必須在開始加電 20ms 內完全達到各自的額定電壓，加電時間應儘可能短。

設計供電順序時必須遵守以下的要求：


- GPU 供電電壓轉換速率符合 50mV/us。
- VDDC 供電時序應先於 VDDCI 或同時供電。
- VDDCI 供電時序應先於 VDDR1 或同時供電。
- VDDC 和 VDD\_CT 不能同時加電；最好一個達到額定值的 90% 後另一個才開始加電。
- DDC/AUX 信號的外部上拉電壓應先於 VDDC 和 VDD\_CT 前完成加電。
- GPU系統圖電時序建議與開機時序圖例



## POWER DOWN SEQUENCE – Mars, Heathrow, Chelsea




<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**


Size <b>C</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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20160508	29	D0601	Del CRT PTN3356 all sheet	Smith

<Variant Name>

		Project Name	Rev
		X505BP	R1.0
Title :			
Size	Dept.: NB-SZ-SYS1		Engineer:
B			
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<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>D</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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<Variant Name>

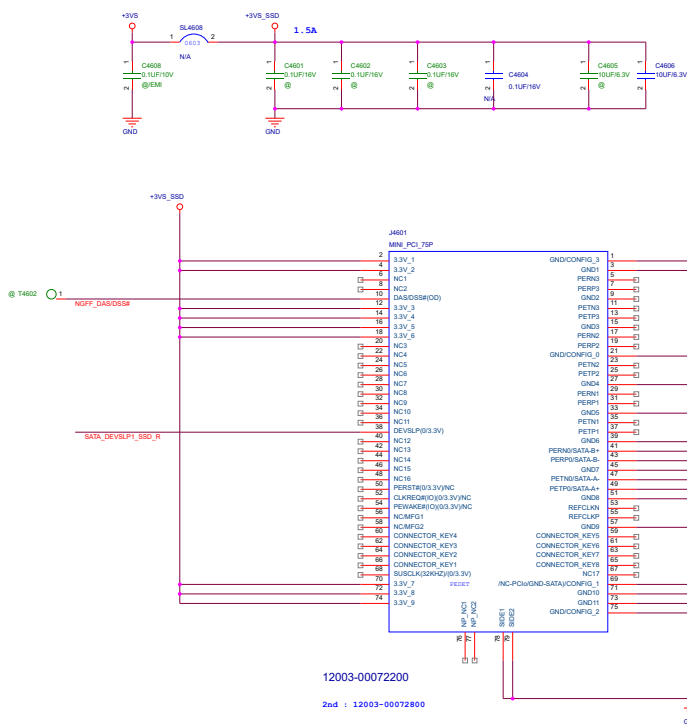
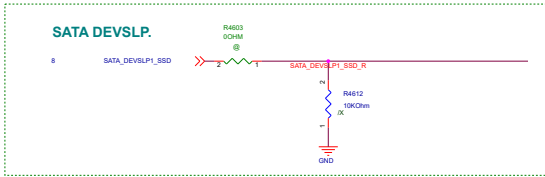
	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>C</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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# SSD CONN.



## 36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express\* Multiplexed Ports

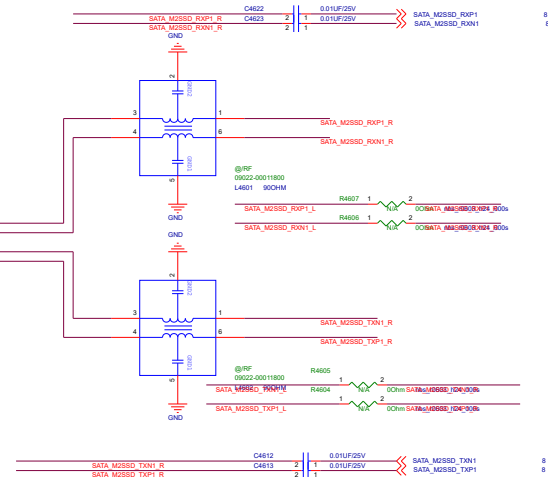
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe\* multiplexed ports.

**Note:**

When SATA and PCIe\* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.


Table 36-7. SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>2</sup>



<Variant Name>

<Variant Name>

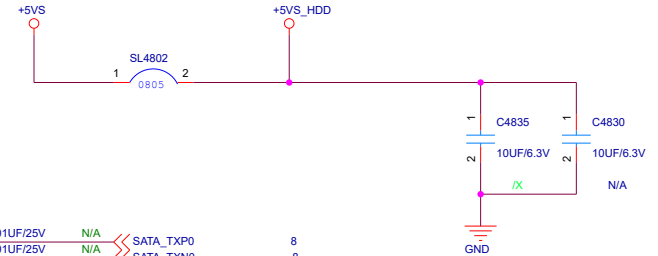
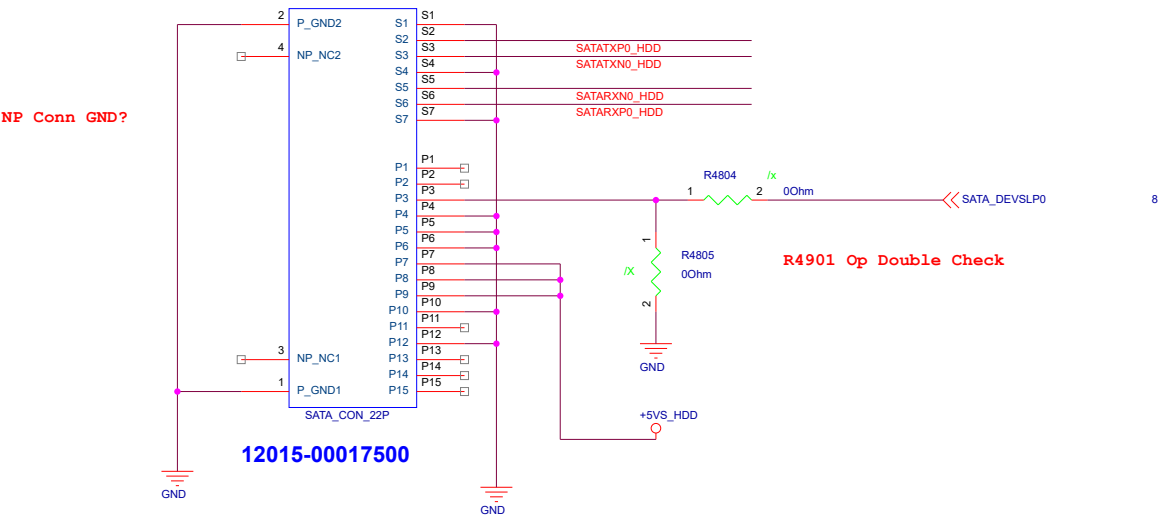
	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

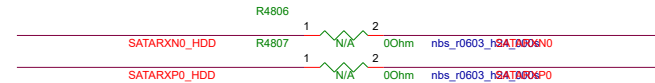
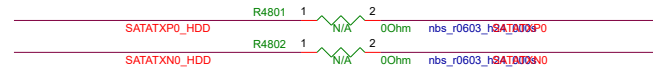
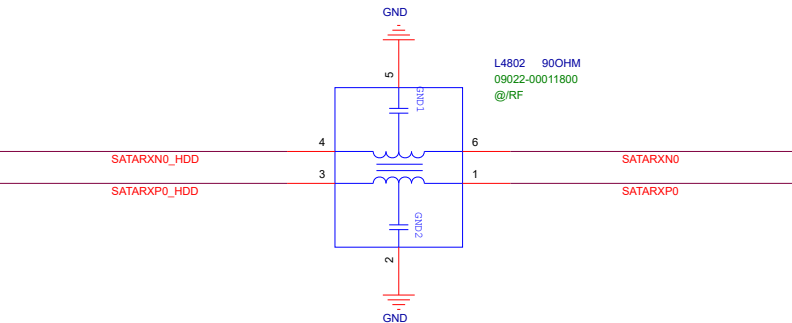
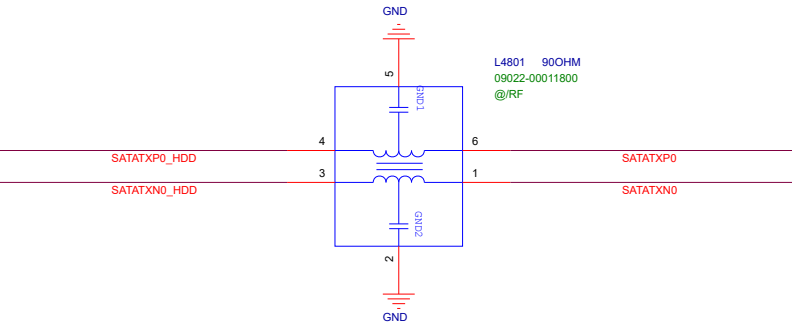
Size <b>B</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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NP Conn GND?




SATATXP0	C4834	2	1	0.01UF/25V	N/A	SATA_TXP0	8
SATATXN0	C4833	2	1	0.01UF/25V	N/A		
SATARXN0	C4831	2	1	0.01UF/25V	N/A	SATA_RXN0	1
SATARXP0	C4832	2	1	0.01UF/25V	N/A		



<Variant Name>



<Variant Name>

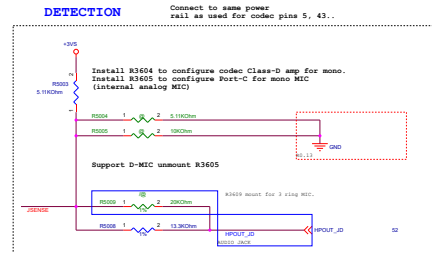
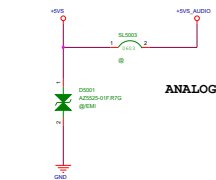
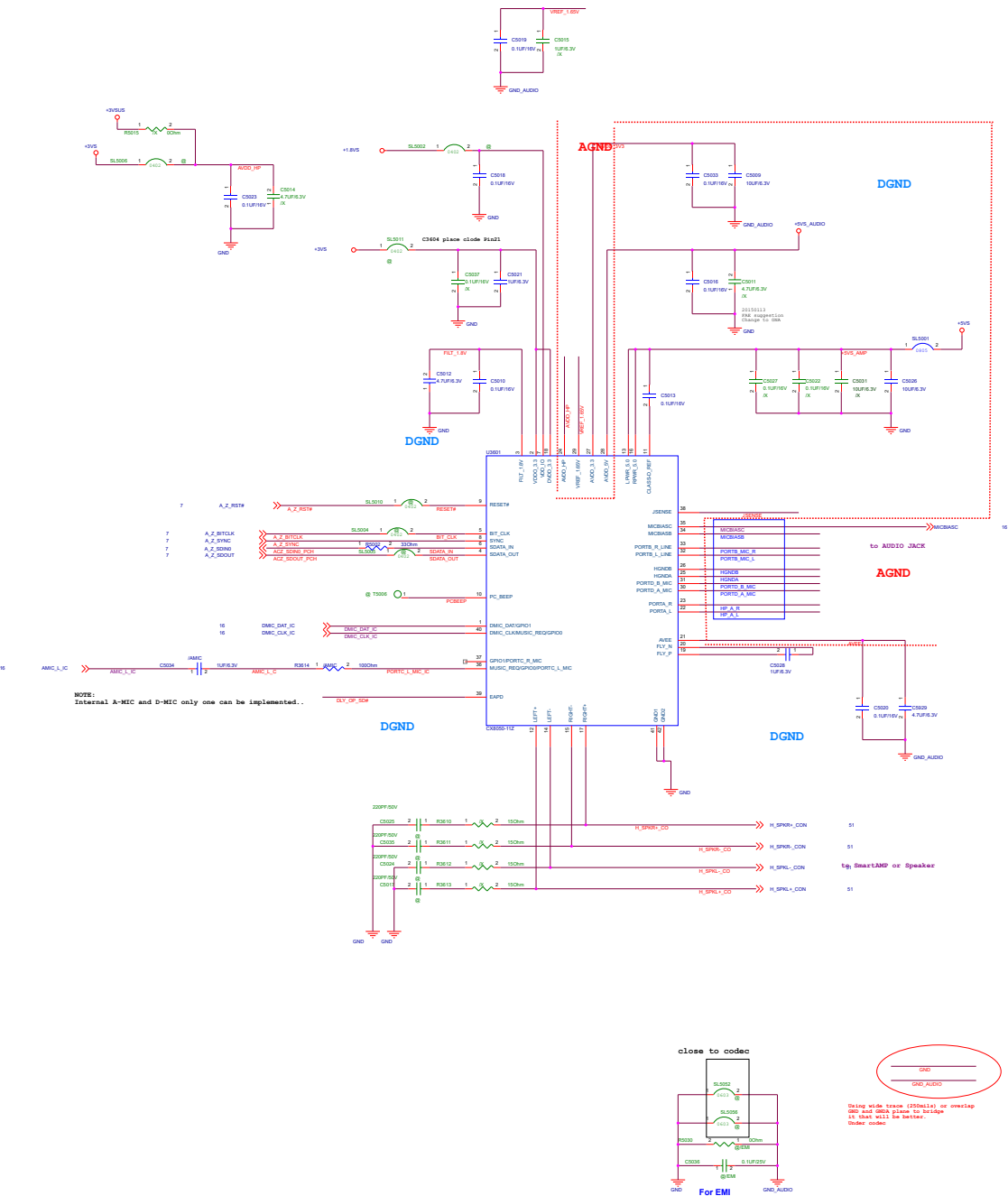
	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>D</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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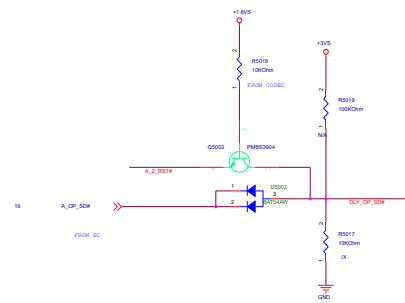
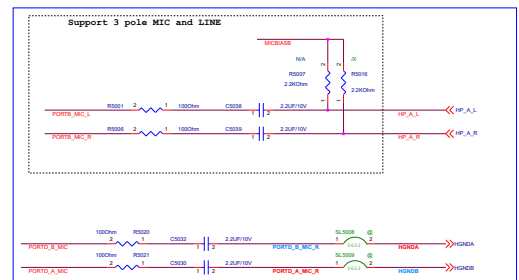
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# AUDIO CODEC (CX8150)

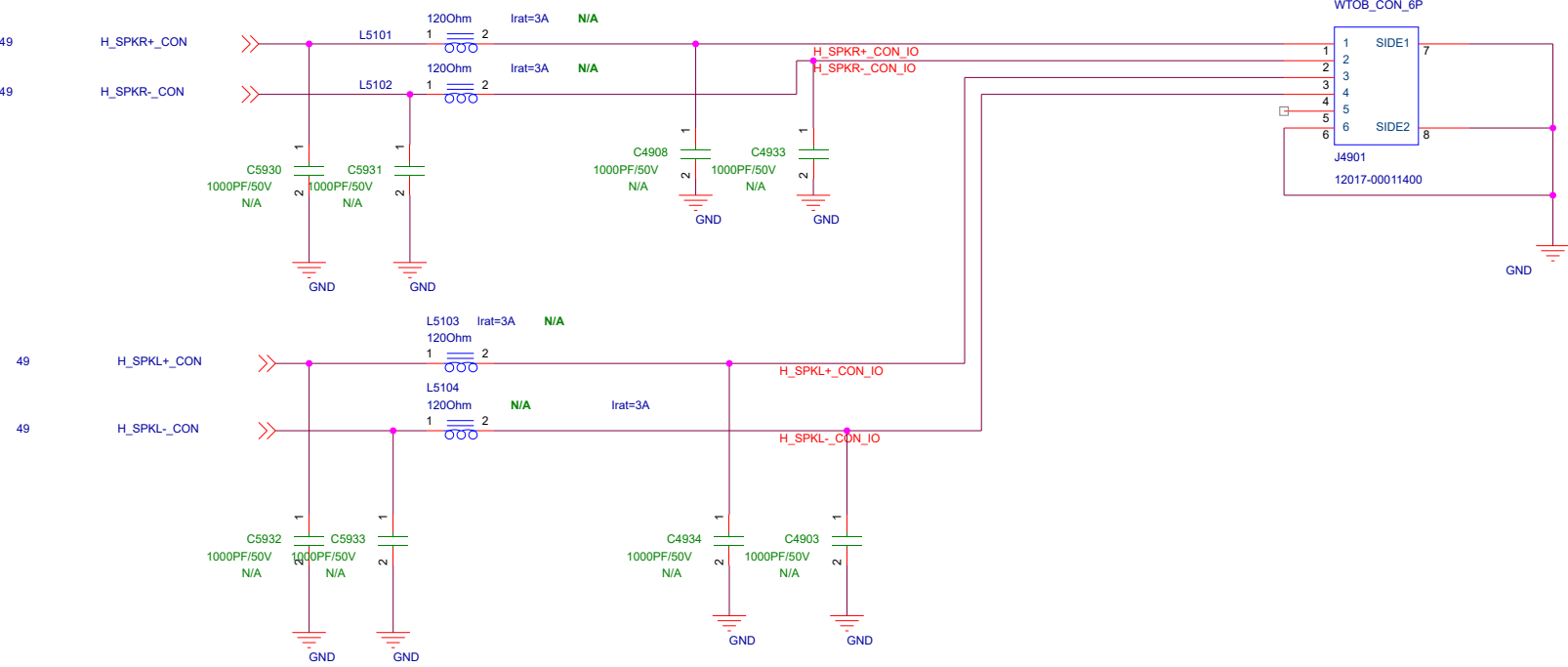


HGND/A/GND  
走線越短越好，線寬盡量>70 mil  
Headphone: Port A  
External MIC: Port B  
Internal MIC: Port C  
Headset: Port A + port D  
Universal Jack : port A + Port B + port D


DGND



Noted Name



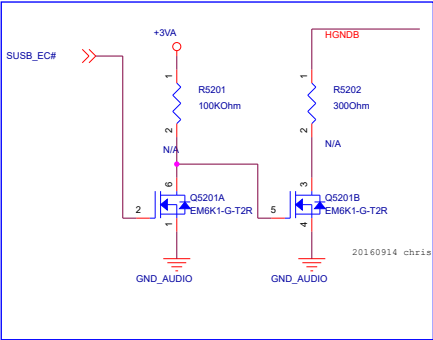
<Variant Name>

		Project Name	Rev
		X505BP	R1.0
Title :			
Size B	Dept.: NB-SZ-SYS1		Engineer:
Date: Thursday, March 30, 2017	Sheet	51	of 99

# MB to IO

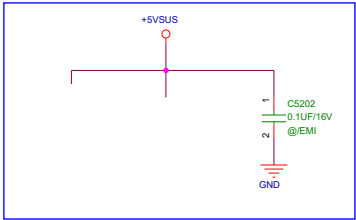
20161031 (follow X456 R1.2 )  
Add Q6801/R6801/R6802/R6803  
for SPK noise issue in 83/84/85

## For AUDIO JACK



20161128 Michael delete R6803

## MB端 (MB to IO)



USB2.0 120 mil 3A

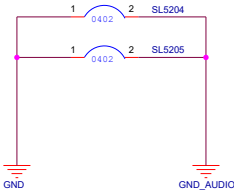
CR 40 mil 0.5A

USB2.0

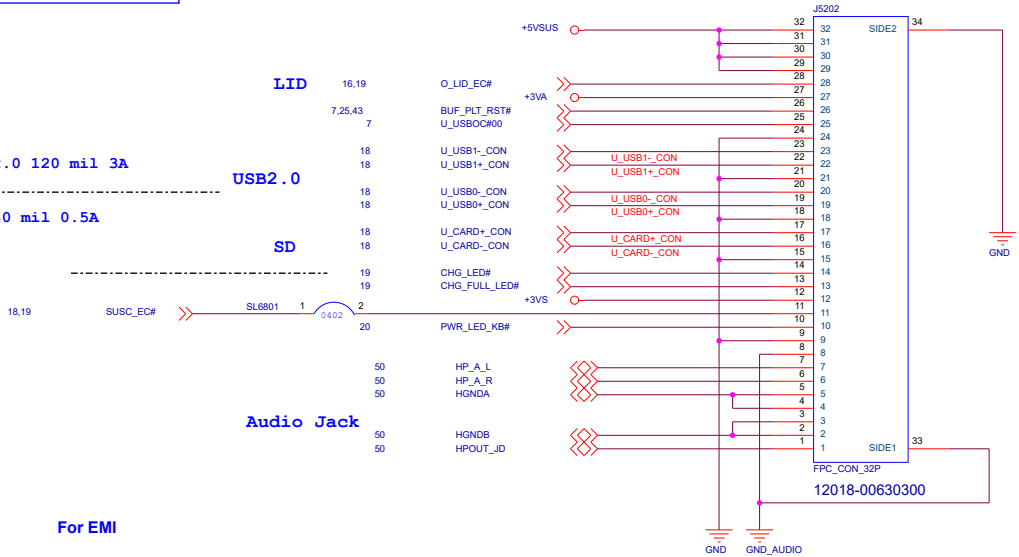
SD

Audio Jack

For EMI



## MB to IO\_B (MB 端)




20161107 Michael  
Change J6802 Conn from 36Pin to 32Pin

<Variant Name>

ASUS		Project Name	Rev
		X505BP	R1.0
Title :			
Size	Dept.:	Engineer:	
B	NB-SZ-SYS1		
Date: Thursday, March 30, 2017	Sheet	52	of 99


<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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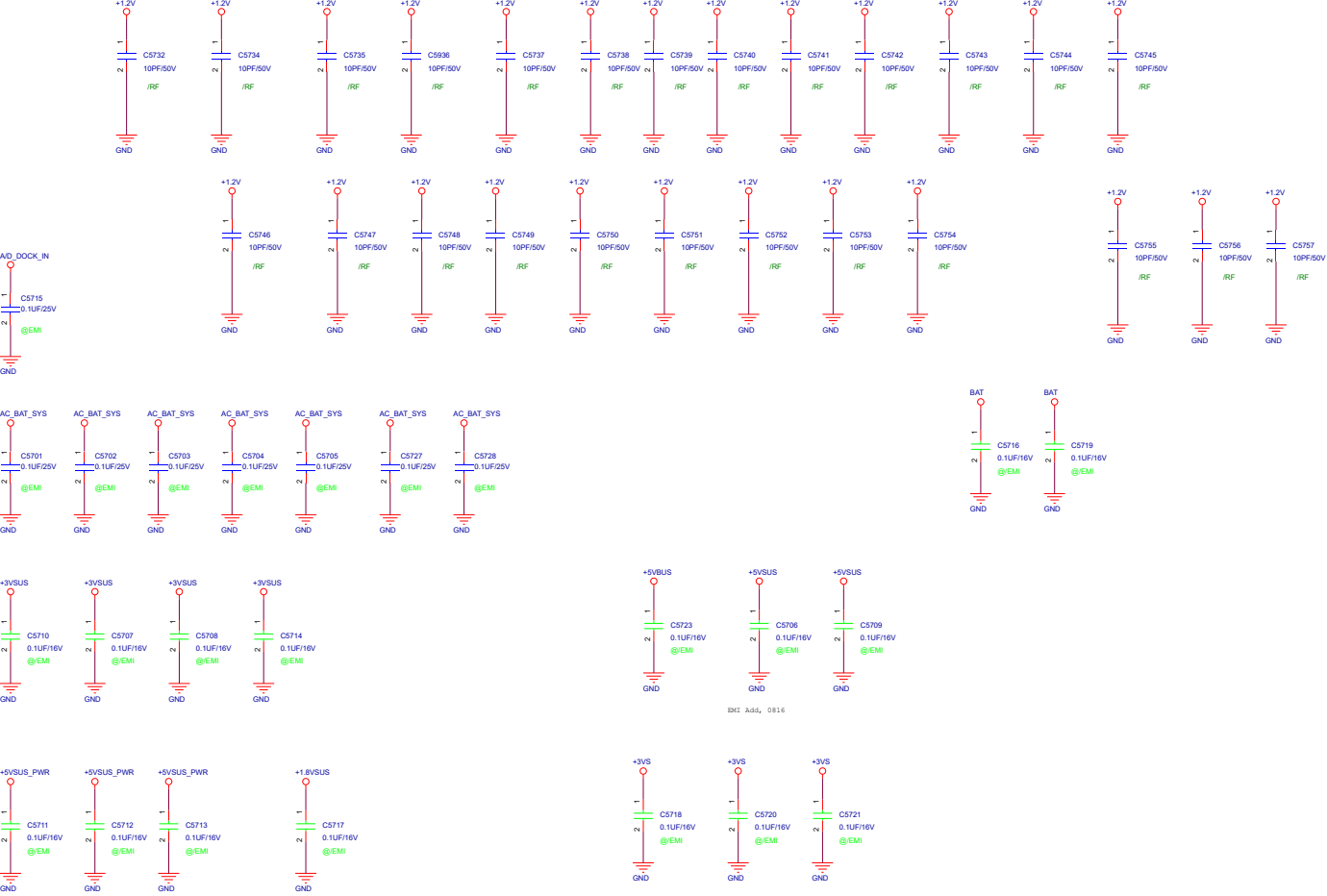
Date: <b>Thursday, March 30, 2017</b>	Sheet <b>55</b> of <b>99</b>
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	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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



















**Title :**

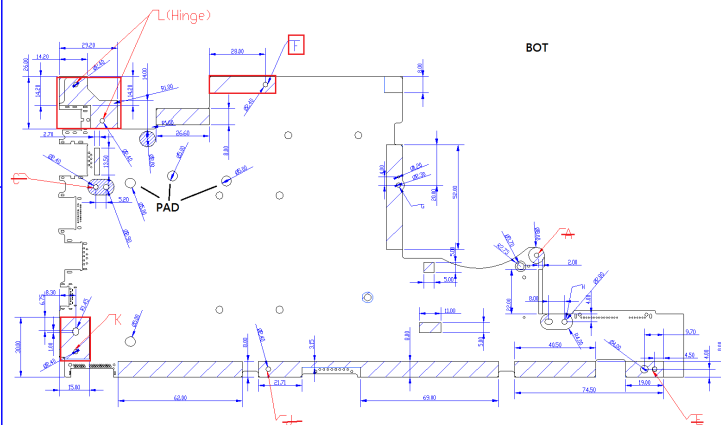
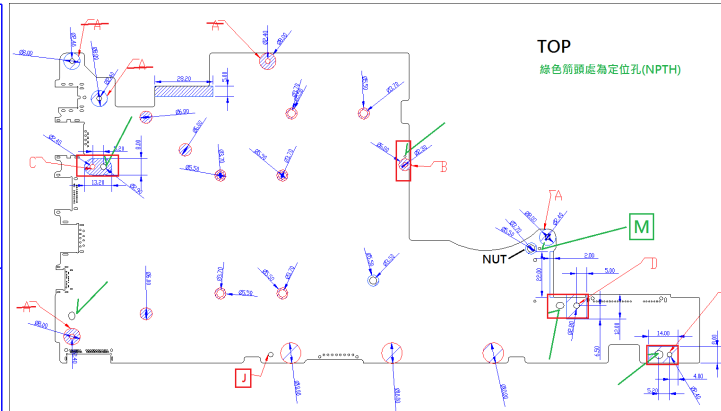
Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Vinafix.com

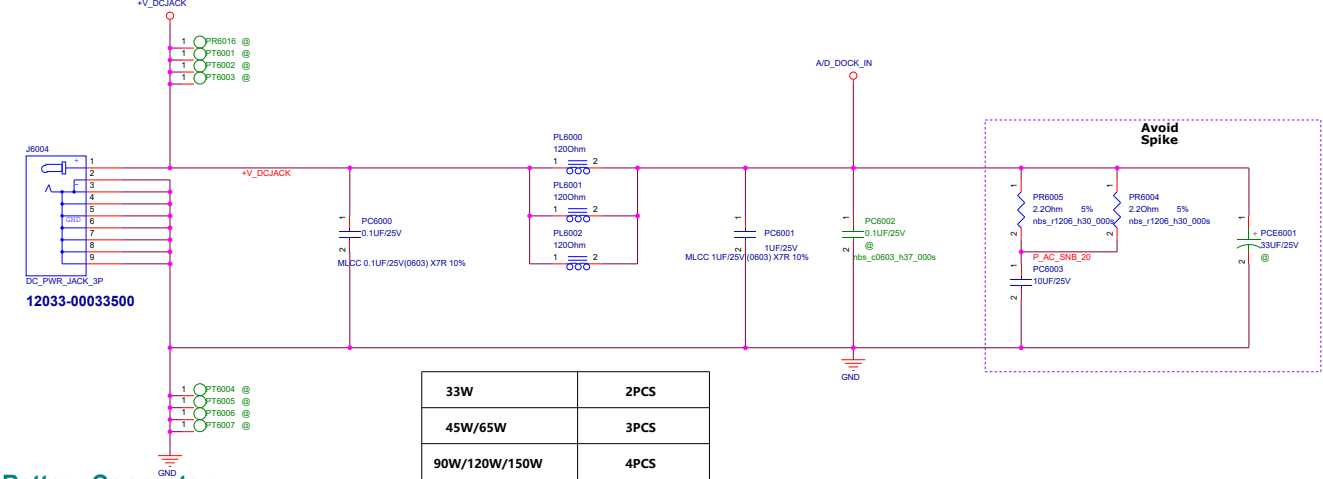
<b>A:1</b> 	<b>M:1</b> 	<b>NUT (BOT)</b> <b>NUT for SSD</b> 	<b>Spring (BOT)</b> 
<b>B:1</b> 	<b>K:1</b> 	<b>L:1</b> 	<b>F:1</b> 
<b>C:1</b> 		<b>NUT (TOP)</b> <b>CPU/VGA NUT</b> 	<b>Gasket (TOP)</b> 
<b>D:1</b> 			
<b>E:1</b> 			
<b>J:1</b> 		<b>NUT (BOT)</b> <b>FAN NUT</b> 	





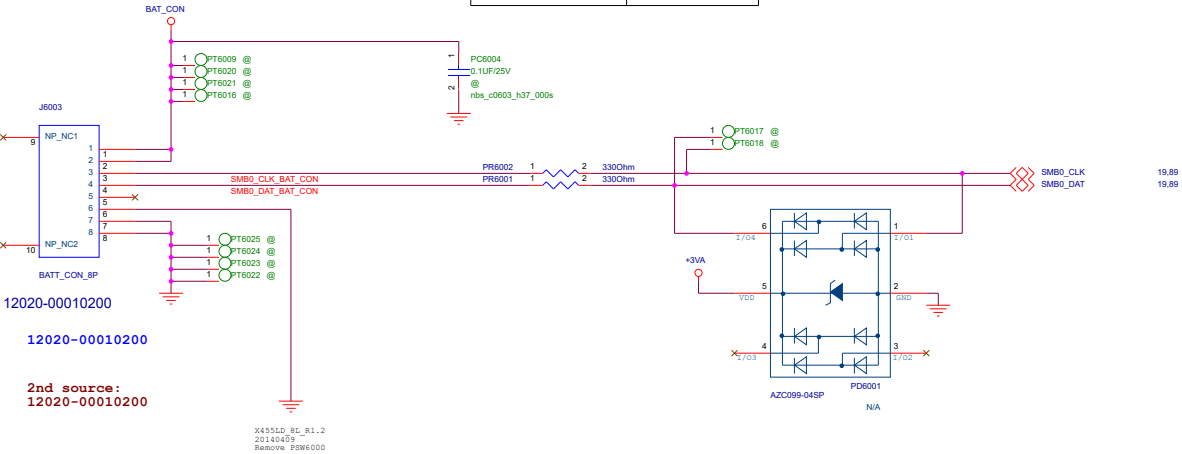
<Variant Name>

		Project Name		Rev
		X505BP		R1.0
Title :				
Size	Dept.: NB-SZ-SYS1			
D	Engineer:			
Date: Thursday, March 30, 2017			Sheet	59 of 99




Battery Connector

33W	2PCS
45W/65W	3PCS
90W/120W/150W	4PCS
180W/230W	6PCS



<Variant Name>		Project Name	Rev
ASUS		X505BP	R1.0
Title : DC & BAT Connector			
Size	Dept.: ASUStek COMPUTER INC. Engineer:		
A3	Date: Thursday, March 30, 2017		
Sheet		60	of 102

<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>61</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>62</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>63</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>64</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>65</b> of <b>99</b>
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<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>66</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>67</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>68</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>69</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>70</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>71</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>72</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>73</b> of <b>99</b>
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<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>74</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>75</b> of <b>99</b>
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<Variant Name>


	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>76</b> of <b>99</b>
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<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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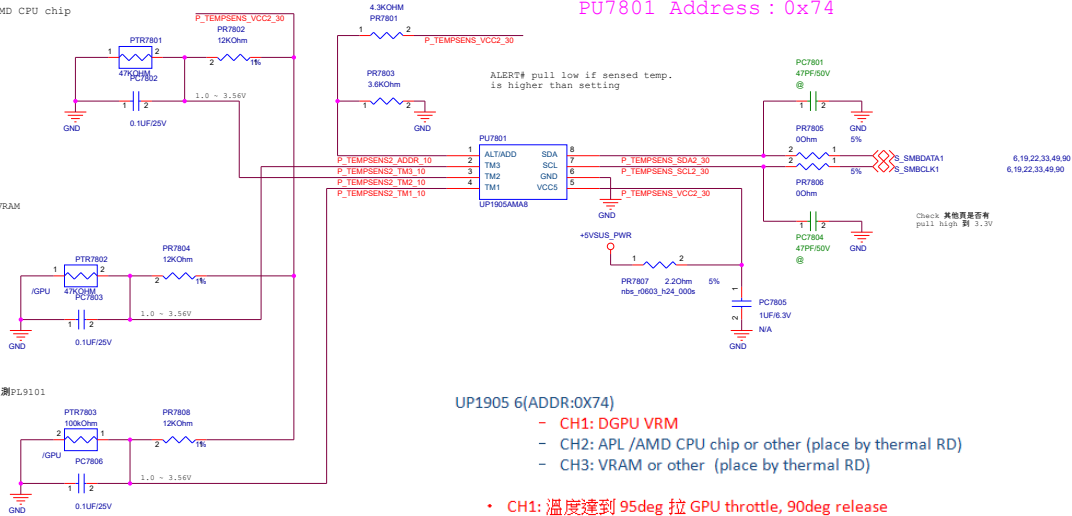
Date: <b>Thursday, March 30, 2017</b>	Sheet <b>77</b> of <b>99</b>
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PTR7801 place near 偵測AMD CPU chip

PU7801 Address : 0x74

PTR7802 place near 偵測GPU VRM

PTR7803 place near 偵測PL9101

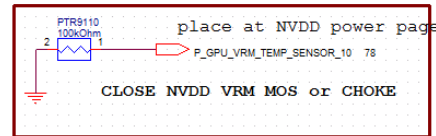


UP1905 6(ADDR:0X74)


- CH1: DGPU VRM
- CH2: APL /AMD CPU chip or other (place by thermal RD)
- CH3: VRAM or other (place by thermal RD)

- CH1: 溫度達到 95deg 拉 GPU throttle, 90deg release
- CH2: 溫度達到 95deg 拉 CPU throttle, 90deg release (by thermal RD modify)
- CH3: 溫度達到 95deg 拉 GPU throttle, 90deg release, (by thermal RD modify)

這顆只有 CH1 的 thermister 放在 PWR NVDD 那一頁(如下),其餘放在 EE 頁面, Ch2,Ch3 擺放位置與 EC 溫度設定點皆由 thermal RD 決定



<Variant Name>

	Project Name <b>X505BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB-SZ-SYS1</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>79</b> of <b>99</b>
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<Variant Name>



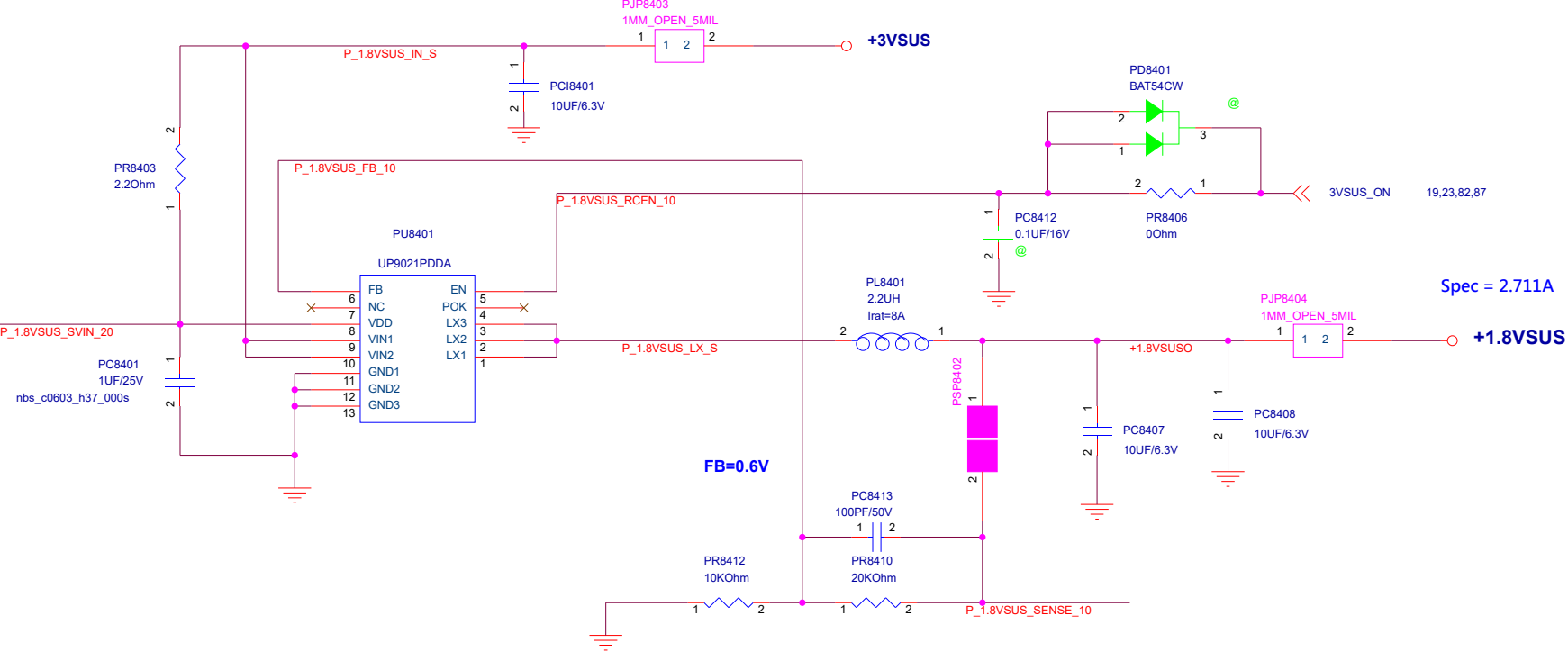


**For UPI DLPM**




Part Reference	UP1565PQKF		UP9002PQKF		RT8248AGQW	
	MLCC	V-CHIP	MLCC	V-CHIP	MLCC	V-CHIP
PR8334	2.2ohm	2.2ohm	10Kohm	10Kohm	@	@
PC8333	1uF	1uF	@	@	0ohm	0ohm
PR8337	@	@	@	@	300Kohm	300Kohm
PR8304	820Kohm	820Kohm	560Kohm	560Kohm	620Kohm	620Kohm
PR8306	178Kohm	402Kohm	100Kohm	@	178Kohm	@
PC8315	820pF	820pF	1000pF	@	820pF	@
PR8301	15Kohm	15Kohm	15Kohm	15Kohm	@	@


<Variant Name>



<Variant Name>

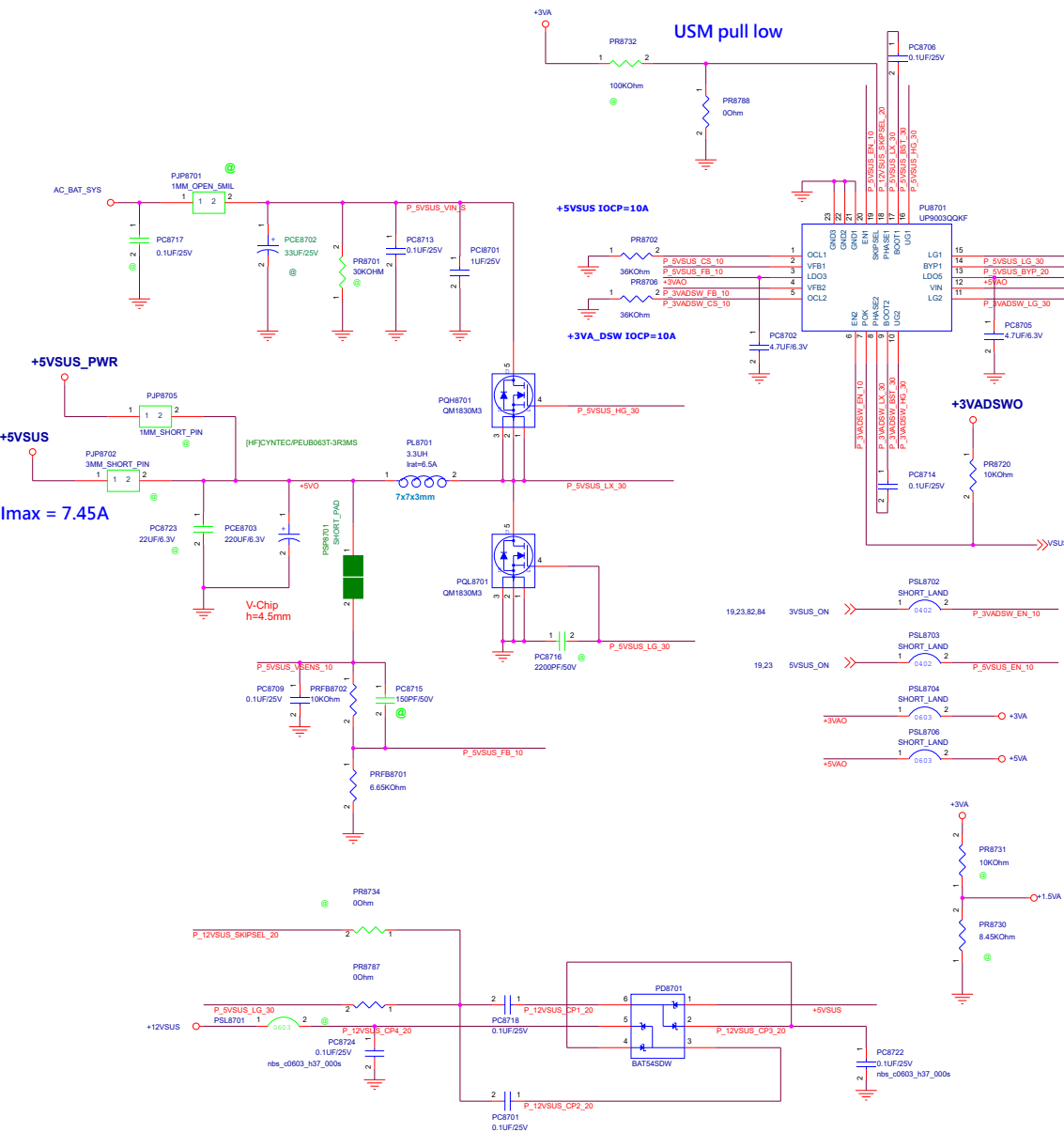
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X505BP			R1.0
Title :			
Size Custom	Dept.: NB Power Team	Engineer:	
Date: Thursday, March 30, 2017	Sheet	84	of 99

<Variant Name>

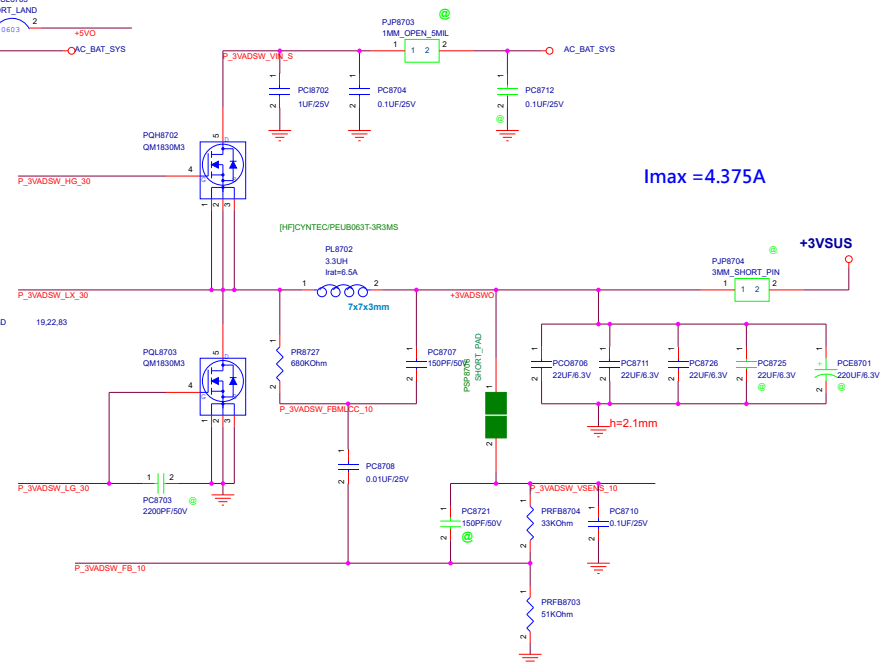
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<b>Title :</b>			
Size  A	<b>Dept.:</b> NB Power Team  <b>Engineer:</b>		
Date: Thursday, March 30, 2017		Sheet	85 of 99



**+3VA\_DSW / +5VSUS [System Power]**

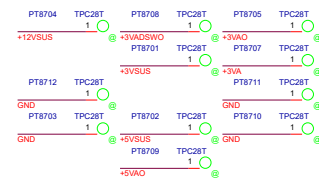


Part Reference	RT8249CGQW		UP9003QQKF	
	MLCC	V-CHIP	MLCC	V-CHIP
PC8707	330pF	@	150pF	@
PR8727	680Kohm	@	680Kohm	@
PC8708	0.01uF	@	0.01uF	@

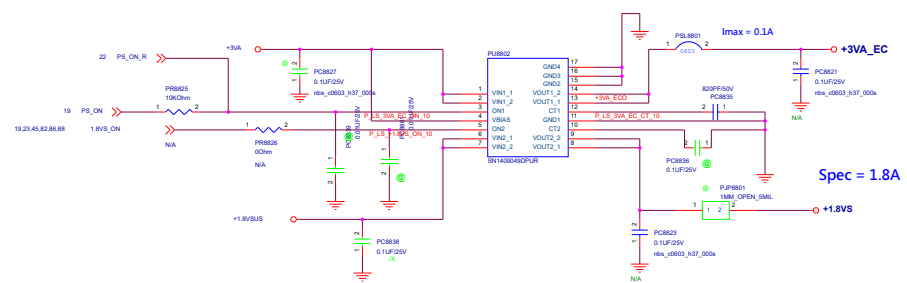
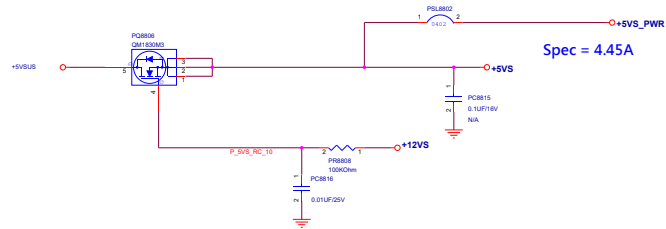
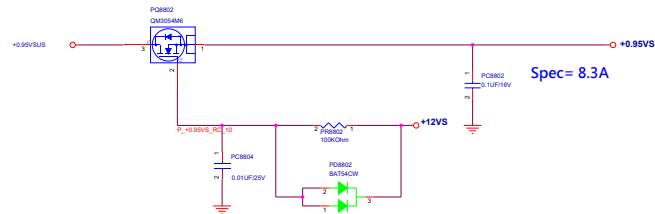
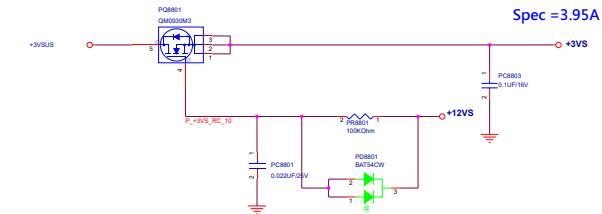


Adaptor Mode (IMVP8)							
	S0	CS	S3	D3S	S4	S5	S5 with USB Chargers
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSV_EC#	1	-	1	-	0	-	0
SUSV_EC#	1	-	0	-	0	-	0

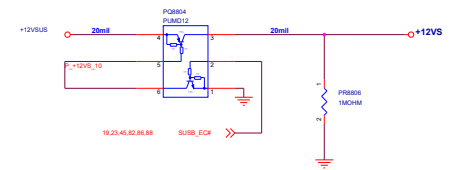
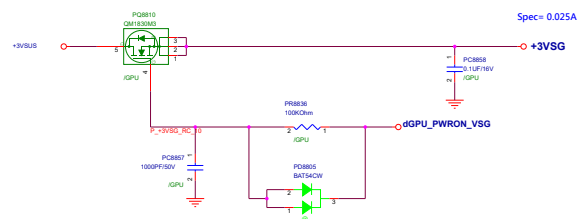
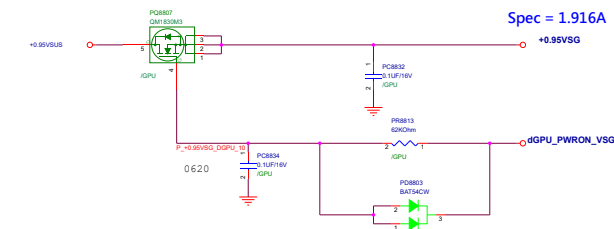
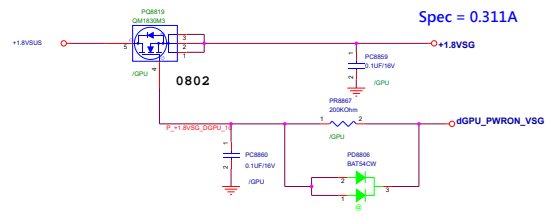
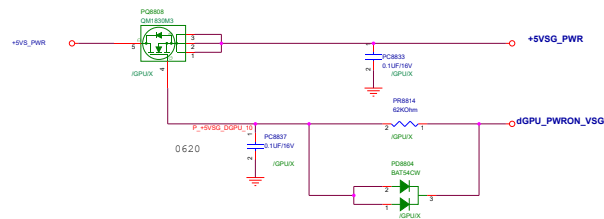
Battery Mode (MVP8)							
	S0	CS	S3	D3S	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



+1.5V , +1.5VS, +0.95VS, 1.8VS, +3VS, +5VS



以下部份，在有DGPU的時候上件



~Blank Name~



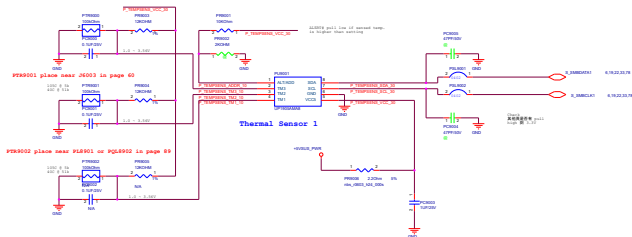
### Address Selection Table

Address	0x70	0x71	0x72	0x73	0x74	0x75	0x76	0x77
000001	000	1 00	00	3 00	3 00	6 00	5 00	00
000005	0000	0 70	0 70	0 00	0 70	3 00	3 70	70

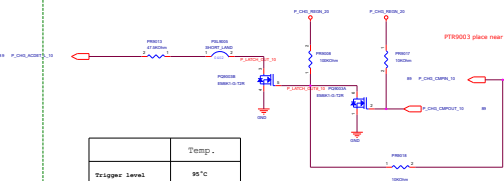
Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
A/G	0	0	0	0	0	0	0
Function	Temp. alarm threshold setting			Send temp. data			bin 4 x 2 bin 3 x 2 bin 4 x 2 When ALARM occurs

VT39100 place near 8Q8901 in page 89



### DC Jack Thermal Latch




	Temp.
Trigger level	95°C
Release level	75°C





<Variant Name>

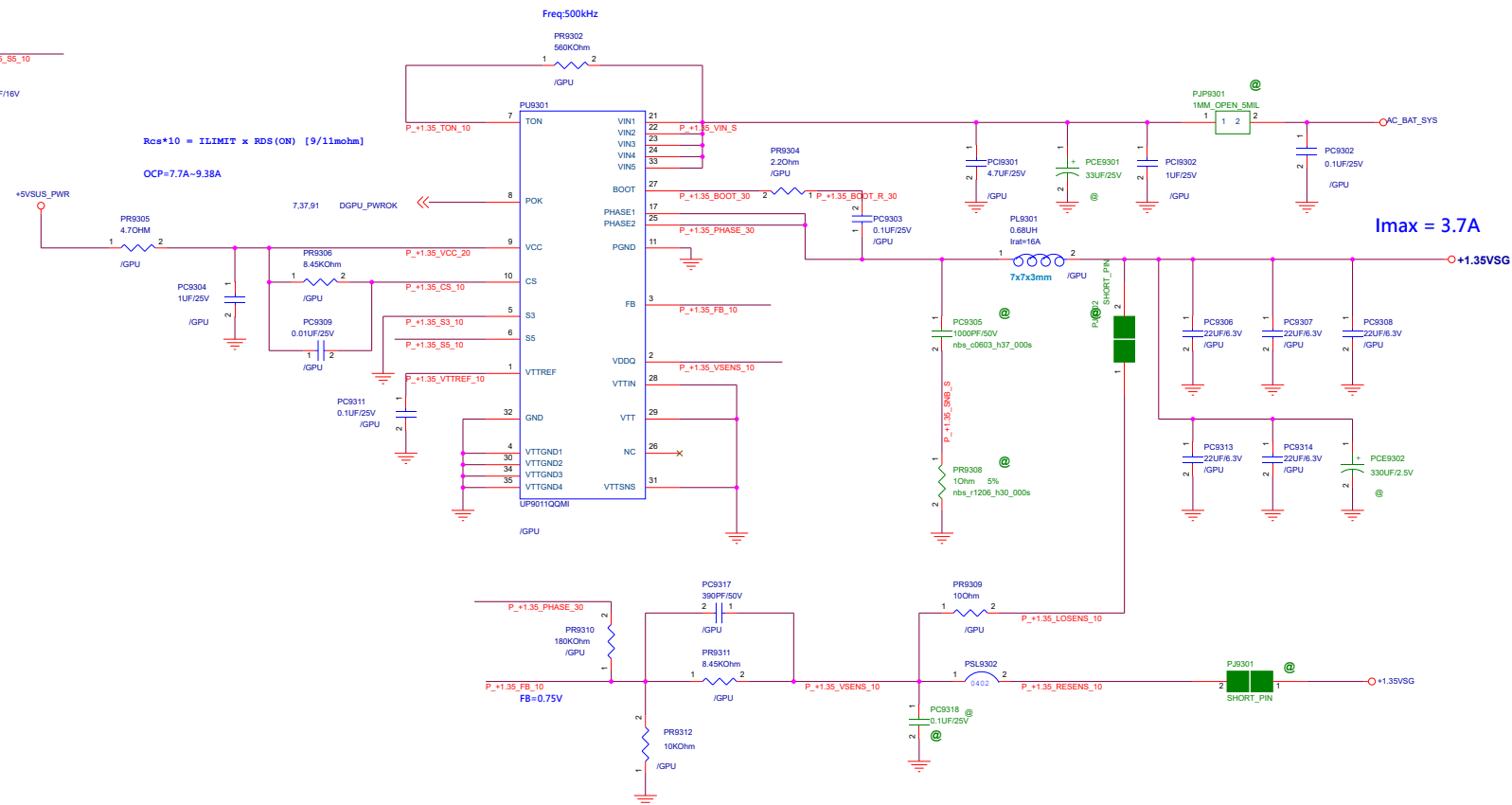
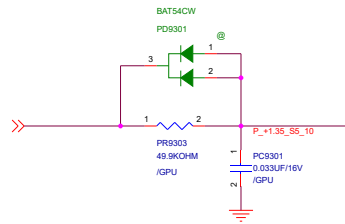
	Project Name <b>E402BP</b>	Rev <b>R1.0</b>
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**Title :**


Size <b>A</b>	<b>Dept.:</b> <b>NB Power Team</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>92</b> of <b>99</b>
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## 37,91 dGPU\_PWRON\_CORE\_EN



		Project Name <b>X505BP</b>		Rev <b>R1.0</b>
<b>Title :</b> <b>PW_+1.35V/+0.675VS</b>				
Size Custom	<b>Dept.:</b> <b>NB Power Team</b>		<b>Engineer:</b>	
Date: <b>Thursday, March 30, 2017</b>		Sheet <b>93</b>	of <b>99</b>	

	Project Name <b>E402BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB Power Team</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>94</b> of <b>99</b>
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<Variant Name>

	Project Name <b>E402BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB Power Team</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>96</b> of <b>99</b>
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	Project Name <b>E402BP</b>	Rev <b>R1.0</b>
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**Title :**

Size <b>A</b>	<b>Dept.:</b> <b>NB Power Team</b>	<b>Engineer:</b>
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Date: <b>Thursday, March 30, 2017</b>	Sheet <b>97</b> of <b>99</b>
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<Variant Name>

		Project Name <b>E402BP</b>	Rev <b>R1.0</b>
<b>Title :</b>			
Size <b>A</b>	<b>Dept.:</b> <b>NB Power Team</b> <b>Engineer:</b>		
Date: <b>Thursday, March 30, 2017</b>		Sheet <b>98</b>	of <b>99</b>



